Neural Recording System with 8 Channel Neural Amplifier and Logarithmic ADC

Chirag Mukesh Mehta, Chaejung Lim, Eric Beauchemin

Abstract—This work proposes a low-power 8 channel neural recording system (NRS) for use in advanced closed-loop neurostimulation applications for the detection and treatment of neurological disorders such as Parkinson’s disease. The analog front end senses and filters the neural activity with eight low-noise pre-amplifiers and band-pass filters. The neural sensing signals are multiplexed to a single logarithmic pipelined ADC. Separation of the low frequency local field potentials (LFPs) from the high frequency neural spikes is done using on-chip finite impulse response (FIR) digital filters. The resulting signals can then be used to dynamically control the neurostimulation parameters in a closed-loop system to alleviate the neurological symptoms of the disease.

Keywords—Neural recording, neurostimulation, logarithmic pipelined ADC, finite impulse response.

I. INTRODUCTION AND MOTIVATION

The accelerating pace of research in neuroscience has created a considerable demand for neural sensing microsystems capable of monitoring the activity of large group of neurons. The ability to record signals from neurons is centered around the electric current flow through the neuron. As an action potential propagates through the cell, the electric current flows in and out of the soma and axons at excitable membrane regions. This current creates a measurable, changing voltage potential within and outside the cell.

This allows for two basic types of recordings. Intracellular recordings occur within the neuron and measure the voltage change with respect to time across the membrane during action potentials. This outputs as spikes through the soma or axon. Another type of recording is the local field potential (LFP), which is an electrophysiological signal generated by the summed electric current flowing from multiple nearby neurons within a small volume of nervous tissue. Voltage is produced across the local extracellular space by action potentials and graded potentials in neurons in the area, and varies as a result of synaptic activity.

Recent research has discovered that these internal neural recordings can provide vital information about the symptoms of various neurological disorders. Consistent excessive power of local field neural potentials at 15-30 Hz are associated with symptoms of Parkinsons Disease in an animal model [1]. Both high-frequency, pulsatile neuronal spike trains and low-frequency continuous LFPs contain important information for closed-loop neurostimulation control [2]. Features of the LFP signals, in particular the energy of LFPs, have emerged as an effective feedback indicator for setting and tuning a Deep Brain Stimulation (DBS) System [3].

Many experiments in non-human primates [4][6] and a pilot clinical trial in a human subject [7] illustrated that control signals directly derived from spiking activities from a population of neurons in the cortical area of the brain can be used to successfully control and manipulate computer devices or robotic limbs. The study in [8] shows that cortical activities from a population of neurons can be used to control even a sophisticated device such as a robotic limb with multiple degrees of freedom. These studies have shown great promise for successful development of practical brain-machine-interface (BMI) systems to restore lost body functions to patients with disorders in the central nervous system such as those suffered because of spinal cord injuries.

In light of the aforementioned motivations, we propose an 8 channel neural recording system, capable of simultaneously recording the local field potentials and the neural spikes, for use in neurological and neurostimulation applications.

II. PRIOR WORK

To avoid the risk of infection, the recording system should be entirely implanted under the skin while the recorded neural data and the power to operate the implant should be transferred through wireless means [9]. This implantability requirement poses major constraints on the size and total power consumption of the recording system [9]. For battery-operated recording systems, low power consumption could prolong the time between recharges, thus expanding the battery’s life to avoid frequent surgeries for battery replacements.

Recently there has been extensive research on developing ICs for acquisition of neural action potentials. In [10], Avestruz et al described a spectral analysis IC for LFP applications, but it relies on off-the-shelf ADC for signal recording, thus making it unattractive for low-power and low-cost applications. Muller et al. [11] presented a DC-coupled neural recording system composed of the ADC, digital lowpass filter and DAC for spike detection. It achieves small area for each channel. However the digital filter is implemented off chip on FPGA making it power hungry.

To record from a large number of cortical neurons, high-channel-count recording systems are needed. Advances in integrated-circuit (IC) fabrication technologies have enabled engineers to increase the number of recording channels that can be put on a single chip by decreasing the size and power consumption per recording channel, while still significantly improving the recording systems performance. The first recording system reported in [12] contained 32 recording channels and data-reduction circuitry while consuming a total power of 5.4 mW (equivalent to 169 μW per channel). Another system...
reported in [13] contained 100 channels and also included wireless data transmission and power-transfer features. By counting only the power consumption from the recording channels and the analog-to-digital converter, the average power consumption of this system is approximately 140 $\mu$W/channel. The system reported in [14] achieved a very low average power consumption of 3.77 $\mu$W/channel. However, due to its very large area per channel, such a system may not be scalable to a high-channel-count system.

For neural neurostimulation and other neurological applications, low power consumption and small area per recording channel are both very important. In this paper, we propose the design of an 8-channel implantable neural recording system for such application with the goal of minimizing the power consumption and the chip area.

### III. OVERALL SYSTEM ARCHITECTURE

Figure 1 shows the overall architecture of our proposed neural recording system. The outputs from the 8 neural amplifiers are multiplexed to the ADC which digitizes its input signal at a rate of 200kS/s. On-chip digital filters separate the neural spikes and the low-frequency field potentials.

#### A. Measurement Electrodes

In the past decade, neuroscientists and clinicians have begun to use implantable MEMS multielectrode arrays to observe the simultaneous activity of many neurons in the brain [15] [16]. These silicon-based electrode structures are inserted into the cerebral cortex to observe the electrical activity of nearby nerve cells. Neural spikes are pulsatile signals with bandwidth of 100 Hz to 10 kHz and amplitude level from 50 $\mu$V to 500 $\mu$V [17]. Local field potentials are continuous, lower frequency signals with bandwidth below 100 Hz, and amplitude levels up to 5 mV [18]. Table 1 below lists the specifications of microelectrodes suitable for various applications [19];

#### B. Low Noise Neural Amplifier

Due to the microvolt level of the neural spikes recorded extracellularly, neural signals must be amplified before spike/LFP detection or digitization can be accomplished. Low amplitude levels further make it necessary to design a neural amplifier with low input referred noise. However, the power restrictions imposed on small implantable devices limit our ability to simply increase the bias currents in order to lower the amplifier noise, especially since the basic amplifier circuit will be repeated many times across the chip. Figure 2 shows the schematic of the neural amplifier, which consists of 3 stages: (i) a front-end amplifier, (ii) a band-pass filter and (iii) a programmable-gain amplifier.

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filter such that the bandwidth of the overall neural amplifier is constant and determined by that of the bandpass filter.

The midband gain of the front-end amplifier is set to 40 dB by capacitive feedback formed by \( C_{\text{in}} \) and \( C_{f} \) around the high gain amplifier \( A_{1} \). Due to the high gain of the front-end amplifier, noise introduced by \( A_{1} \) determines the noise performance of the overall amplification. The input-referred noise power per unit bandwidth of \( A_{1} \), which consists of both thermal and flicker (1/f) noise components, can be expressed as: \([21][22]\)

\[
V_{\text{in,1}}^{2} = \frac{4kT}{g_{m1}} \left[ \frac{2K_{p}}{W_{1}L_{1}C_{ox}^{2}} + \frac{2K_{n}}{W_{1}L_{1}C_{ox}^{2}} \right] g_{m2}^{2} + \frac{1}{\alpha^{2}} \left( \frac{kT}{g_{m1}} \right)^{2} \frac{1}{g_{m1}}
\]

where \( g_{m2} \) is the transconductor of the \( i^{th} \) transistor in the OTA, \( K \) is the inverse of the subthreshold slope, \( k \) is the Boltzmann constant, \( T \) is the absolute temperature, \( C_{ox} \) is the oxide capacitance per unit area, and \( K_{p} \) and \( K_{n} \) are the technology dependent 1/f noise coefficients of the pMOS and nMOS respectively. The factor \( \alpha \) represents the ratio of the effective transconductance of the OTA (\( G_{m} \)) and the transconductance of \( M_{1} \) and \( M_{2} \) (\( g_{m1} \)) and can be approximated as: \([21]\)

\[
\alpha \approx \frac{g_{so}}{g_{so} + g_{ds1}/(g_{s5}/\epsilon_{05} + g_{ds1}/g_{s3}/\epsilon_{03})}
\]

The outputs from the eight low noise amplifiers are multiplexed through an analog multiplexer and input to the ADC.

The outputs of the eight low noise amplifiers are multiplexed through an analog multiplexer and input to the ADC. Figure 5 shows the schematic of the analog multiplexer. The core of the analog multiplexer consists of eight source-follower drivers formed by the transistors \( M_{11}, M_{12}, M_{21}, M_{22}, M_{31}, M_{32}, M_{41}, M_{42} \). The source-follower drivers buffer the amplifiers’ outputs \( V_{out,i} \) to provide low output impedance necessary to drive the input capacitance of the ADC. Multiplexing of the amplifiers’ outputs is achieved through the switches \( S_{1}, S_{8} \). When switch \( S_{i} \) (\( i = 1,2, \ldots, 8 \)) is closed, \( V_{out,i} \) is buffered and multiplexed to the input of the ADC. Only one of the switches \( S_{1}, S_{8} \) is closed at any given time. The duration for which each switch is closed is chosen such that it suffices the ADC’s sampling duration.

**TABLE I: Summary of Neural Recording Parameters for Different Applications**

<table>
<thead>
<tr>
<th>Neural Signal</th>
<th>Measurement Technique</th>
<th>Amplitude</th>
<th>Bandwidth</th>
<th>Electrodes</th>
<th>Chronic Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Extracellular Action Potentials</td>
<td>Voltage Amplification</td>
<td>50 to 500 ( \mu )Vpp</td>
<td>100 Hz to 200 Hz</td>
<td>Metal/silicon microelectrode</td>
<td>High</td>
</tr>
<tr>
<td>Intracellular Action Potentials</td>
<td>Voltage Amplification</td>
<td>10 to 70 mVpp</td>
<td>1 mHz to 200 Hz</td>
<td>Glass microproptette</td>
<td>Very low</td>
</tr>
<tr>
<td>Local Field Potentials</td>
<td>Voltage Amplification</td>
<td>0.5 to 5 mVpp</td>
<td>1 mHz to 200 Hz</td>
<td>Metal/silicon microelectrode</td>
<td>High</td>
</tr>
<tr>
<td>Electroencephalogram</td>
<td>Voltage Amplification</td>
<td>1 to 10 mVpp</td>
<td>1 mHz to 200 Hz</td>
<td>Surface electrode</td>
<td>Very high</td>
</tr>
<tr>
<td>Ionic Current</td>
<td>Patch Clamping</td>
<td>1 to 10 nA</td>
<td>1 mHz to 10 kHz</td>
<td>Glass microproptette</td>
<td>Low</td>
</tr>
<tr>
<td>Redox Current</td>
<td>Amperometry</td>
<td>100 fA to 10 ( \mu )A</td>
<td>100 Hz to 10 kHz</td>
<td>Iridium oxide/carbon fiber microelectrode</td>
<td>High</td>
</tr>
</tbody>
</table>

**Fig. 4: Schematic of the programmable gain amplifier**

Figure 4 shows the schematic of the programmable gain amplifier (PGA). The gain of the PGA can be programmed to any of the ‘\( n \)’ values and is given by \( A_{n} = 1 + (R_{f}/R_{D_{i}}) \), \( i = 0,1,2, \ldots, n \), where \( R_{D_{i}} \) is the total resistance seen between the negative input terminal of \( A_{2} \) and node \( V_{x} \) when the switch \( D_{i} \) is closed. The decoder ensures that only one of the switches \( D_{i} \) can be closed at a given time depending on the decoder’s input. The amplifier \( A_{2} \) is designed using a standard two-stage Operational Amplifier topology with Miller compensation. The class AB output buffer, similar to the one used in figure 2(b) can be included to drive resistive loads (feedback resistors at the output of \( A_{2} \)).

**C. Analog Multiplexer**

The outputs from the eight low noise amplifiers are multiplexed through an analog multiplexer and input to the ADC. Figure 5 shows the schematic of the analog multiplexer. The core of the analog multiplexer consists of eight source-follower drivers formed by the transistors \( M_{11}, M_{12}, M_{21}, M_{22}, M_{31}, M_{32}, M_{41}, M_{42} \). The source-follower drivers buffer the amplifiers’ outputs \( V_{out,i} \) to provide low output impedance necessary to drive the input capacitance of the ADC. Multiplexing of the amplifiers’ outputs is achieved through the switches \( S_{1}, S_{8} \). When switch \( S_{i} \) (\( i = 1,2, \ldots, 8 \)) is closed, \( V_{out,i} \) is buffered and multiplexed to the input of the ADC. Only one of the switches \( S_{1}, S_{8} \) is closed at any given time. The duration for which each switch is closed is chosen such that it suffices the ADC’s sampling duration.
D. Logarithmic Pipelined ADC

To save area and power consumption, a high dynamic range logarithmic ADC is used. Logarithmic encoding is well suited and efficient for neural signals since a high dynamic range can be represented by a short word length. The advantage of a logarithmic ADC is that larger signals levels are more tolerant of noise, allowing larger quantization errors for larger values. Hence, as shown in the example in figure 6, a moderate resolution log ADC can sense both small and large signals, while a moderate-resolution linear ADC can detect only large signals [2].

If we assume an N-bit logarithmic ADC with an input voltage $V_{in}$, a full-scale input range $V_{range}$, a log base B, and output digital bits $b_{N-1}, b_{N-2}, ..., b_0$, then the transfer function of the ADC is given by: [23]

$$2^N \log_B (B \cdot V_{in}/V_{range}) = b_{N-1}2^{N-1} + ... + b_0$$  \hspace{1cm} (1)

where $[x]$ denotes the largest integer which is not larger than $x$. As the input amplitude increases, the quantization becomes coarser. The LSB size is given by:

$$\text{LSB} = V_{range} \cdot (B^{1/2^N} - 1)/B$$  \hspace{1cm} (2)

The dynamic range (DR) is defined as the ratio of the input range to the smallest resolvable signal, and is expressed as:

$$\text{DR} = V_{range}/\text{LSB} = B/(B^{1/2^N} - 1)$$  \hspace{1cm} (3)

From equations (2) and (3) we see that the dynamic range DR increases as the base of the logarithmic function, B, and the resolution, N, increase. A logarithmic ADC has a higher dynamic range than a conventional linear ADC of the same resolution. An ADC with a dynamic range of 54dB is enough to cover the entire range of spikes and LFPs, considering both the microelectrode noise and the background cortical activity noise [24]. Thus, from equations (2) and (3), we have chosen $B=10$ and $N=7$ for this work. An additional bit represents the sign of input; hence the overall ADC resolution is 8bits with one sign bit and seven magnitude bits.

A simplified block diagram of the 8-bits pipelined log-ADC is shown in figure 7.

The sign of the input is determined first. If the sign of input is negative, the input will be inverted since log functions can only operate on positive inputs. After sign detection, the input is processed through a Sample and Hold Amplifier (SHA), five 1.5-bit log-ADC stages, and a 2bit flash-ADC final stage. The single-ended to differential output SHA is shown in figure 8 and the 2bit flash-ADC stage is shown in figure 9.
A digital correction block collects the digital bits and assembles the 8-bit output. A direct logarithmic implementation of the 1.5 bit per stage pipeline requires squaring to replace the multiplication-by-2 operation in a linear domain pipeline and conditional multiplication to replace the conditional addition or subtraction. Figure 10 explains the conditional multiplication scheme and shows the scaling of the reference voltages and the multiplication gains for the different stages. To avoid analog squaring, the reference voltages for the comparators and the gain settings are scaled in order to achieve the same result as squaring the output of each 1.5 bit stage [25].

Table I gives the reference voltage values and the gains for each stage. \( V_{\text{ref}0,j} \) is the lower threshold and \( V_{\text{ref}1,j} \) the upper threshold for stage \( j \). These differential threshold voltages are generated on-chip and share a 600 mV common-mode voltage. \( G_0,j \) is the highest gain setting, and is selected when the stage input is less than \( V_{\text{ref}0,j} \). \( G_1,j \) is the midrange gain for the stage inputs that locate between \( V_{\text{ref}0,j} \) and \( V_{\text{ref}1,j} \). \( G_2,j \) is the bypass gain for the stage inputs larger than \( V_{\text{ref}1,j} \) for the \( j \)th stage [2].

### Table II: Voltage Reference and Gain Settings in the Logarithmic 8-Bit ADC with \( B=10 \)

<table>
<thead>
<tr>
<th>Stage (j)</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{ref}0,j} ) (mV)</td>
<td>142</td>
<td>292</td>
<td>419</td>
<td>501</td>
<td>548</td>
<td>568</td>
</tr>
<tr>
<td>( V_{\text{ref}1,j} ) (mV)</td>
<td>253</td>
<td>389</td>
<td>484</td>
<td>539</td>
<td>568</td>
<td>579</td>
</tr>
<tr>
<td>( V_{\text{ref}2,j} ) (mV)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>589</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>( G_{0,j} )</td>
<td>1.02</td>
<td>1.28</td>
<td>1.74</td>
<td>1.15</td>
<td>1.075</td>
<td>-</td>
</tr>
<tr>
<td>( G_{1,j} )</td>
<td>1.78</td>
<td>1.43</td>
<td>1.15</td>
<td>1.075</td>
<td>1.037</td>
<td>-</td>
</tr>
<tr>
<td>( G_{2,j} )</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-</td>
</tr>
</tbody>
</table>

The proposed design is a 22-tap finite impulse response (FIR) digital filter. Unlike an analog filter, a digital filter can easily implement higher order filtering but with an extremely low power consumption, especially for low-frequency signals [26]. Also, a digital filter is programmable and its operation can be adjusted without modifying the hardware.

The proposed design is a 22-tap finite impulse response (FIR) Butterworth filter shown in figure 12 [27]. Each unit delay represents a latch. The coefficients represent the multipliers. The adders are used to combine the digital values.
Coefficients will be calculated using the standard `fir1` function in Matlab. `fir1` uses windowing to select FIR coefficients designed to keep the response as ideal as possible. The sampling frequency for filtering is same as the ADC sampling frequency of 200kHz. The output of the ADC is fed to both the low pass and high pass butterworth filters which separate the LFPs and neural spikes respectively.

IV. PERIPHERAL CIRCUITY

Power can be provided to the chip inductively via an off-chip 5-mm gold-on-polyimide coil [28]. The chip contains a fully-integrated bridge rectifier based on the design by [29], eliminating the need for off-chip diodes. A voltage reference circuit and a voltage regulator provide a steady 3.1V DC supply for the digital and analog circuits on chip. Two off-chip capacitors are needed: one to resonate with the power coil, and another large-valued capacitor to smooth out the unregulated DC supply after rectification. Commands are sent to the chip by amplitude modulating the inductive power signal. On-chip circuits recover this data as well as a system clock from the AC power signal.

A. Voltage Reference Circuit

The principle of our voltage reference circuit is shown in figure 13. The bias voltage subcircuit accepts current $I_P$ through the pMOS current mirrors and produce an output voltage (i.e. the reference voltage) $V_{REF}$. The bias voltage subcircuit consists of a transistor $M_4$ and two source-coupled pairs $M_3-M_6$ and $M_5-M_7$. All the MOSFETs except for $M_{R1}$ are operated in the subthreshold region. The MOS resistor $M_{R1}$ is operated in a strong-inversion, deep-triode region. The reference voltage generated by the circuit is equal to the threshold voltage of the transistors [28]. A variable gain voltage regulator can be used to increase the voltage up to the desired value of 3.1V and to ensure that a constant voltage is supplied irrespective of the current drawn by the load.

B. Clock Generation Circuit

The clock generator consists of a clock recovery circuit with a frequency divider to generate the timing logic for the digital circuitry in the neural recording system.

C. Data Transmission Circuitry

The chip continuously generates the LFPs and neural spikes data for all the electrodes. This data must be transmitted out of the body wirelessly. To accomplish this, a fully integrated FSK transmitter, similar to the one used in [13] can be realized. The operating frequency must be chosen below 1 GHz to minimize the attenuation of high frequencies by the tissue and to operate near the FCC-approved MICS (Medical Implant Communication System) band at 402-405 MHz.

V. COMPARISON WITH STATE-OF-THE-ART

Table III shows the comparison of the proposed neural recording system with state of the art.

<table>
<thead>
<tr>
<th>Application</th>
<th>Recording</th>
<th>Recording</th>
<th>Recording</th>
</tr>
</thead>
<tbody>
<tr>
<td>Position of Electrodes</td>
<td>Cortex</td>
<td>Cortex</td>
<td>Cortex</td>
</tr>
<tr>
<td>LNA Channels</td>
<td>32</td>
<td>128</td>
<td>8</td>
</tr>
<tr>
<td>LNA Gain</td>
<td>39.5 dB</td>
<td>40 dB</td>
<td>40 dB</td>
</tr>
<tr>
<td>LNA Pass Band</td>
<td>100 Hz</td>
<td>0.1 Hz</td>
<td>15 Hz</td>
</tr>
<tr>
<td>to 7 kHz</td>
<td>to 20 kHz</td>
<td>to 10 kHz</td>
<td></td>
</tr>
<tr>
<td>LNA Power/Channel</td>
<td>13.68 uW</td>
<td>23.9 uW</td>
<td>9 uW</td>
</tr>
<tr>
<td>Input Referred Noise</td>
<td>3.35 uVRms</td>
<td>4.9 uVRms</td>
<td>5 uVRms</td>
</tr>
<tr>
<td>Filters</td>
<td>Analog</td>
<td>Analog</td>
<td>Analog + Digital</td>
</tr>
<tr>
<td>ADC</td>
<td>Extended Counting</td>
<td>5/10k</td>
<td>Log Pipeline</td>
</tr>
<tr>
<td>Resolution</td>
<td>13 bits</td>
<td>6 to 9 bits</td>
<td>8 bits</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>512 kS/sec</td>
<td>640 kS/sec</td>
<td>200 kS/sec</td>
</tr>
<tr>
<td>Total Power</td>
<td>11 mW</td>
<td>6 mW</td>
<td>5 mW</td>
</tr>
<tr>
<td>Process Technology</td>
<td>0.5 um</td>
<td>0.35 um</td>
<td>0.5 um</td>
</tr>
</tbody>
</table>

The bias voltage subcircuit accepts current $I_P$ through the pMOS current mirrors and produce an output voltage (i.e. the reference voltage) $V_{REF}$. The bias voltage subcircuit consists of a transistor $M_4$ and two source-coupled pairs $M_3-M_6$ and $M_5-M_7$. All the MOSFETs except for $M_{R1}$ are operated in the subthreshold region. The MOS resistor $M_{R1}$ is operated in a strong-inversion, deep-triode region. The reference voltage generated by the circuit is equal to the threshold voltage of the transistors [28]. A variable gain voltage regulator can be used to increase the voltage up to the desired value of 3.1V and to ensure that a constant voltage is supplied irrespective of the current drawn by the load.

The circuit consists of a current source subcircuit and a bias-voltage subcircuit. The current source subcircuit is a modified $\beta$ multiplier self-biasing circuit that uses a MOS resistor $M_{R1}$ instead of ordinary resistors. It generates a current $I_P$.

VI. WORK DISTRIBUTION

The work distribution amongst the team members is illustrated in table IV.
TABLE IV: Work Distribution

<table>
<thead>
<tr>
<th>Member</th>
<th>Tasks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chirag Mukesh Mehta</td>
<td>Neural Amplifier, BPF, Programmable gain amplifier</td>
</tr>
<tr>
<td>Chaung Lim</td>
<td>Logarithmic Pipelined ADC</td>
</tr>
<tr>
<td>Eric Beauchemin</td>
<td>Analog multiplexers, biasing circuits, digital filters</td>
</tr>
<tr>
<td>All three</td>
<td>Layout of the ADC</td>
</tr>
</tbody>
</table>

REFERENCES


