A Dry Electrode Low Power CMOS EEG Acquisition System on Chip for Seizure Detection
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Abstract—This paper describes a low power EEG acquisition system on chip adapted for the use of dry electrodes to acquire signals suitable for seizure detection. The System on Chip consists of a High Pass Filter, a Low Noise Amplifier, a Low Pass Filter, an ADC driver and an ADC. The ADC output is then carried to a wireless processor where signals in a specific frequency range are analyzed for seizure detection.

Keywords—Dry electrode, Impedance boosting, ADC, Seizure detection, choppers, electroencephalography.

I. INTRODUCTION

Great progress has been made in treatments dedicated to patients suffering with neurological conditions like epileptic seizures. It is crucial to develop new systems that will allow us to acquire neural signals and analyze them to find a correlation between these signals and the clinical symptoms [1]. This paper describes a non-invasive system on chip that extracts an analog EEG and converts it in the digital domain for analysis through machine learning algorithms. In current EEG monitoring systems, wet electrodes are a limitation due to the reduction of the impedance of the skin-electrode interface and the creation of a discomfort for the patient. Dry electrodes introduce a gel-free solution but require circuit modifications to counter the increase of impedance between the skin-electrode interface [2]. EEG has the advantage to be non-invasive and changes in the signal that happen seconds before the clinical symptoms can be detected to warn the patient or to trigger the recording of EEG for analysis by a neurologist. Machine learning algorithms are used for each patient to determine if the signal is a seizure EEG or a non-seizure EEG. Our work will be focused on the acquisition part of the system on chip by extracting and converting the EEG to a digital signal for the processing by the processor. The device is also intended to be used in a wireless environment so reception and transmission antenna systems will be part of the device but won’t be designed in this project.

II. SYSTEM BLOCK DIAGRAM

The proposed recording system consists of an analog front-end circuit including chopper-stabilized low noise amplifier, high and low pass filters, an ADC driver and a SAR ADC. Figure 1 shows the top-level block diagram. The integrated peripheral circuits include a bandgap circuit, two linear voltage regulators for separate analog and digital power supplies, and a current reference circuit to provide bias currents throughout the entire chip. Alimentation is provided by a lithium polymer battery; its durability will depend on the power consumption of the chip. It will be wireless rechargeable thanks to induction. The MCU provides the clock to ADC to easily program the ADC sampling frequency and the chopping frequency for the LNA. The MCU process the data extracted from the ADC and send them via wireless connection to the patient’s phone and to a clinical center.

III. DESIGN SPECIFICATIONS

A. Body-Electrode Interface

The electrode model used is the dry-contact which is equivalent to the circuit represented in Figure 2, where the resistor and capacitance in parallel represent the Stratum Corneum (surface skin) and the resistor represents the body [3]. EEG signals from the electrode are between 10 and 50 uV. Electrode Offset Voltage (EOV) is expected to be high (10-100 mV). A high pass cut-off is used to reject EOV while passing low frequency EEG [1].

B. Chopper-stabilized LNA

Recording of low amplitude and relatively low-frequency EEG signals require minimization of the effects of intrinsic and popcorn noise sources from the active components. This excess noise can artificially depress the signal-to-noise ratio (SNR) and lead to incorrect diagnostic conclusions. Chopper stabilization allows to mitigate 1/f noise with low power consumption [1]. We have chosen to use a fully differential approach for the chopper-stabilized LNA to offer more noise.
and interference immunity. However, two challenges associated with chopper amplifiers are how to reduce their output ripple and residual offset.

1) Ripple reduction

The output ripple is due to the amplifier’s up-modulated offset voltage. Compared to the level bio potential signals, the ripple can be quite large and can limit the amplifier’s output headroom. Many prior designs address the output ripple by employing feedback to null the ripple [10]. In [11], foreground calibration is performed to generate a compensating current using a digital-to-analog converter to cancel the offset, and this current is fed to the output of gm1. However, these designs add power consumption. By placing a DC-blocking impedance between the first stage and the second stage (Fig.3), the opamp DC offset and flicker noise do not appear at the output. To ensure stable DC biasing, a large duty-cycled resistor Rf is placed across the first operational amplifier stage. This ripple rejection technique is analyzed in [12]. The schematic for the fully differential chopper amplifier is given Fig. 4.

![Fig. 3. Two stage fully differential chopped amplifier with ripple rejection](image)

![Fig. 4. Schematic of the fully differential amplifier](image)

2) DC servo loop

The residual output offset is caused by the spikes of the input chopper, which in return are due to the charge injection mismatch of the switches. The spikes are demodulated by the output chopper and the result is a residual output offset. The residual offset can be compensated by a DC servo loop with filter which will also be used for the second pole of the high pass filter [13] (Fig.5).

3) High Pass Filter

The EEG signal bandwidth is in the range 0.5-100 Hz, so the first stage is designed as a high pass amplifier with a cut-off frequency close to 0.1 Hz. The high pass cut-off frequency is widely implemented using a pseudo-resistor larger than 100 GΩ in the feedback loop [13]. However pseudo-resistors limit the linearity of the front-end to 8 bits. Also, pseudo-resistors are very sensitive to process variations and their resistance can vary by a factor of 100. These issues make pseudo-resistors unreliable in a clinical setting [13]. Therefore, to realize large linear resistors, pseudo-resistors are replaced with duty-cycled resistors to enable high linearity and reliability (Fig. 5) [13]. The poles of the high pass filter are provided by the Chopper amplifier and the DC servo loop (Fig. 5).

4) Impedance Boosting

Considering the impedance introduced by the electrode, the input impedance of our current amplifier should be much larger to avoid signal attenuation [1]. Chopping reduces the DC input impedance of the sensing front-end. The low input impedance can generate offset currents that can cause tissue damage. To increase the input impedance, a capacitive impedance boosting loop can be used [2]. However, the boost impedance with the DC servo loop is not well suitable to increase the impedance. A new input-impedance boosting technique has been introduced in [13]. The auxiliary-path used charges the input caps Cin at the beginning of every chopping phase using aux-buffers (Fig. 5), reducing the charge provided by the input Vel to zero, thus boosting Zin. However, a positive feedback loop is formed around the aux-buffers, leading to the aux-buffer DC offset and flicker noise (modeled by Voff) being amplified and appearing. Such large offsets, if left unchecked, can saturate the front-end. In [14] Voff is up-modulated to fc/4 by using mixers M1 and M2 (Fig. 6), where fc is the chopping frequency. Therefore, Voff creates a benign ripple instead of a DC offset at Vel.

![Fig. 5. Schematic of the chopped-stabilized LNA](image)

Storage capacitors Caux=8pF assist the aux-buffers at the beginning of the pre-charge phase (Fig. 6) by charge-sharing with Cin, and are disconnected for the remainder of the pre-charge phase. It leads to higher input impedance without increasing power consumption [14].

![Fig. 7. Auxiliary path with aux-chopping and pre-charge assistance for boosting impedance](image)
5) **Chopper-stabilized LNA**

The targeted chopper-stabilized LNA specifications are given in Table 1.

<table>
<thead>
<tr>
<th>Metrics</th>
<th>Target Specification</th>
</tr>
</thead>
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<tr>
<td>Voltage Supply</td>
<td>1.2V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>~10µW</td>
</tr>
<tr>
<td>DC Input impedance</td>
<td>~1GΩ</td>
</tr>
<tr>
<td>Input-referred noise</td>
<td>~6µV</td>
</tr>
<tr>
<td>Ripple rejection</td>
<td>yes</td>
</tr>
</tbody>
</table>

**Table 1. Chopper-stabilized LNA Specifications**

6) **Low pass filter and ADC driver**

The low-pass filter and single differential converter have a much smaller impact than the CS-LNA on the noise and instrumentation issues. Together, their power is approximately 20% of the total instrumentation amplifier power [1]. Given the characteristics of EEG signals (0.5Hz – 100 Hz), the low pass filter provides two poles near 200Hz. This filter will use an OTA with a standard two-stage topology. The purpose of the low pass filter is to provide frequency cut-off for the EEG signals but also additional gain to the system. An example schematic for the low pass filters is shown in Fig. 8.

**Fig. 8. Low Pass Filter Schematic**

Each low pass filter will provide a gain 20dB and a cut-off frequency at -3dB equal to 200Hz. The filter is built around a two stage OTA with a differential stage and a buffer stage.

We use an additional gain and buffer block before the ADC input. The ADC processes signal differentially and is robust to any common-mode errors. Differential ADC also achieves superior linearity and better matching against process variations than the single-ended version. This block has also been designed to drive the capacitive sample-and-hold of the ADC. The topology uses two OTAs, each with a differential input stage and a buffer output stage to drive high resistors. The gain at each output is around 6dB. The OTAs used consist of a differential and a buffer stage. The schematic for this block is shown in Fig. 9.

**Fig. 9. Gain stage and ADC driver**

**C. Analog-to-Digital Converter**

1) **General structure**

For seizure onset detection, ADC resolution of at least 12 bits is required [4]. SAR ADCs are quite popular with the neural sensing applications and could be a good profile for our requirements [5].

The ADC used in the system is thus a 12-bit successive approximation register converter. A block diagram is shown in Fig. 10: it uses a 6-bit main-DAC and a 6-bit sub-DAC architecture [6], both implemented as passive charge-redistribution capacitor arrays, which provide an inherent sample and hold function.

An important feature of the ADC for this application is that it maintains its energy per conversion down to very low speeds (i.e., 600 S/s).

**Fig. 10. ADC Block Diagram**

A controlled power-gating ensures that the static biasing remains on for only the minimum time required by the conversion. The ADC is fully differential, which helps achieving 12-bit dynamic range for the given noise floor and provides power-supply noise rejection, since supply noise originating from capacitor array switching is an important concern.

The conversion plan of this ADC is shown in Fig. 11: it starts by purging the DAC capacitors so that they can be used
to derive a suitable auto-zeroing reference. Additionally, the auto-zeroing and sampling operations are separated. Consequently, sampling is delayed with respect to the start of the conversion. This delay is undesirable in some applications. However, purging, auto-zeroing, and sampling in separate phases improve the common-mode rejection, low-voltage operation, and noise performance of the ADC.

Fig. 11. ADC Conversion plan

2) DAC Circuits

The sampled common-mode affects the DAC output common-mode during bit-decisions. For proper offset cancellation in the comparator preamplifiers, however, it is critical that the DAC common-mode be equal to the auto-zeroing reference voltage. No differential-mode error is observed if the input common-mode equals the auto-zeroing reference. However, if the input common-mode deviates by even a few hundred millivolts, mismatch results in a differential current through the preamplifier input devices, causing a large differential-mode voltage error of several millivolts at the output.

First, as shown in Fig. 12(a), the capacitor arrays are purged of previous charge by shorting their top and bottom plates. Then, as shown in Fig. 12(b), they are switched so that an appropriate auto-zeroing reference can be generated for the comparator. Finally, input sampling is performed.

During sampling, which is shown in Fig. 12(c), the top-plates of the differential capacitor arrays are shorted, and their voltage simply floats to the input common-mode. Since only one switch is required to decouple the positive and negative arrays, the charge injection errors in this network are not subject to switch mismatch. Constituent pMOS and nMOS devices are sized so that the total switch impedance is symmetric about the common-mode voltage expected during differential sampling (i.e., mid-V_{ref}). Consequently, the top-plate sampling switch sees a well-matched impedance on either side, and its channel charge distributes equally. An advantage of this sampling network is that, since half the input is sampled on each array, the DAC outputs always remain within the rails [7].

Fig. 12. DAC arrays during (a) purging, (b) auto-zeroing and (c) sampling

More importantly, however, the top-plate voltage floats to the input common-mode, and, consequently, as desired, only the differential-mode input signal gets sampled. Sampling only differential-mode charge guarantees that the DAC output voltage during critical bit decisions will always be centered around midscale. Hence, to avoid differential mode errors in the preamplifiers due to device mismatch, the auto-zeroing voltage should also be at midscale. This voltage must be generated prior to sampling by switching the purged capacitor arrays into the divider configuration shown in Fig. 12(b).

3) Comparator

A block diagram of the comparator used is shown in Fig. 13: it has three cascaded preamplifiers. The preamplifier circuit has a nominal gain of 3.

Fig. 13. Comparator block diagram

Since the first preamplifier is noise limited, a bandwidth limiting output capacitor is used to manage its SNR, giving this stage the longest time-constant and greatest power consumption. However, all the preamplifier bias currents have been minimized, and, due to parasitics, the delays of even the later stages are sizeable. Under these circumstances reducing the gain requirements of the entire cascade saves considerable power [6].
We want the relative offsets of the ADC to be small. Accordingly, offset cancelled preamplifiers can be used to obtain a signal swing beyond the latch offset. In this design, however, to maximize the comparator efficiency, an offset compensating latch is used. Thus, even in the presence of severe mismatch, the swing requirement at the output of the preamplifiers is just a couple of millivolts.

4) **SAR Algorithm**

The SAR ADC operation is illustrated in Fig. 14. The conversion starts with setting the MSB to 1. The resulting DAC output is then compared to input signal. If input signal is higher than DAC output, the MSB is kept as one and otherwise it is set to 0. In the next clock cycle, the second significant bit is compared in the same way and is accordingly. This is continued till the last bit.

![Fig. 14. SAR algorithm for a 4-bit ADC](image)

5) **SAR Logic Block**

A simple SAR logic block can be developed using D flip-flops. For an N-bit ADC, we will require 2N*D+1 flip-flops. The schematics of the SAR logic block and shift the registers are shown in Fig. 15. In the beginning of the conversion cycle, all flip-flops except X13 are set to state 0. X13 is set to state 1. X13 sets the output of X1 to 1. After comparing this digital code to the input signal, the comparator output sets X1 as explained in the previous section. The second shift register goes high in the second cycle and sets X2 to 1. X2 also serves as the clock signal for X1. This action is repeated till the LSB is decided. Once the conversion is over, the end of conversion (EOC) bit goes high.

![Fig. 15. SAR logic block](image)

6) **ADC Specifications**

The targeted ADC specifications are given in Table 2.

<table>
<thead>
<tr>
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<td>Resolution</td>
<td>12 bits</td>
</tr>
<tr>
<td>Maximum Sampling Rate</td>
<td>100kS/s</td>
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<tr>
<td>Power consumption</td>
<td>200nW @ 500S/s</td>
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<td>INL</td>
<td>0.19LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>0.16LSB</td>
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<tr>
<td>ENOB</td>
<td>10.55</td>
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<tr>
<td>SNDR (at Nyquist)</td>
<td>65dB (f&lt;sub&gt;N&lt;/sub&gt;=50kHz)</td>
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**TABLE 2. ADC Specifications**

D. **Voltage references**

1) **Bandgap voltage reference**

The bandgap voltage reference is designed to provide a constant voltage Vref to our system independent of the power supply voltage Vdd and the temperature. The bandgap reference is formed using a diode-referenced self-biasing circuit (CTAT), a thermal voltage-referenced self-biasing circuit (PTAT) and the required start up circuit. The reference voltage is the sum of the PTAT and CTAT voltage drops. The schematic of the adopted circuit is shown in Fig. 16 [9].

![Fig. 16. Bandgap voltage reference](image)

For our system, we will be designing the bandgap voltage reference to generate Vref equal to 1.3V, for a supply voltage Vdd of 5V. The generated voltage reference will supply power to the different blocks and reference current.

2) **Voltage regulator**

In addition to the bandgap reference voltage circuit, a voltage regulator is added at the output of the BGR to ensure a constant voltage across the system. The voltage regulator uses a unity gain amplifier with negative feedback to output 99% of the input reference voltage. The schematic for the voltage regulator is shown in Fig. 17.
IV. **SYSTEM LEVEL SIMULATION**

We ran system level simulations for a few blocks of our system using ideal operational amplifiers for most of them. System level simulations helped us define values and metrics for several parameters like the gain and cut-off frequencies of the low pass filters, ADC driver and supply voltage generated by the voltage references.

1) **Low Pass filter**

For this simulation, we used the schematic shown in Fig. 18. The amplifier used is an ideal operational amplifier with a linear gain of 120dB. We ran an AC Sweep simulation to get the output transfer function. The gain of the low pass filter is set at 20dB in the flat region with a cut-off frequency of 166 Hz at -3dB. Fig. 19. shows the output of the low pass filter in dB versus the frequency.

2) **ADC Driver**

The ADC driver has been simulated using the same ideal operational amplifier as in the low pass filter simulation. This block will provide us with an additional gain of 6dB and the ability to drive the input sample and hold capacitors of the ADC. Fig. 20. shows the schematic of the ADC driver and Fig. 21. displays the achieved 6dB gain for each one of the differential output.

3) **Bandgap reference voltage**

The bandgap voltage reference simulation has been implemented at transistor level. The transistors used are ideal and only the length and width parameters have been changed to achieve the desired results. Fig. 22. shows the schematic for the bandgap reference voltage circuit. We ran a DC sweep simulation to output the evolution of the reference voltage depending on the supply voltage Vdd. Results of the simulation are shown in Fig. 23. For a supply voltage Vdd of 5V, the generated reference voltage is equal to 1.32V.
Fig. 22. Bandgap reference voltage schematic

Fig. 23. Reference voltage evolution versus supply voltage

V. STATE OF THE ART

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<tr>
<td>$Z_{in}$</td>
<td>&gt;700MΩ</td>
<td>&gt;3.5GΩ</td>
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<td>&gt;1GΩ</td>
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<td>Input referred noise</td>
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<td>0.205μVRMS</td>
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TABLE 3. Comparisons with previous works

VI. TASKS TO BE COMPLETED

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<td>Voltage and current references</td>
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<tr>
<td>Integration</td>
<td>Valentin Béranger, Karim Eloueldhiri, Matthieu Durbec</td>
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TABLE 4. Distribution of tasks

REFERENCES


