

Design of a Low Power Low Noise System-on-Chip for ECG Monitoring and Diagnostic

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Abstract—A system-on-chip for the application of Electrocardiogram (ECG) monitoring and diagnostic is proposed in this paper, which includes reference circuit, instrumentation amplifier (IA), band-pass filter (BPF), amplifier stage and successive approximation register analog-to-digital converter (SAR-ADC). The Common-Mode Rejection Ratio (CMRR) of IA is greater than 132.87 dB, total gain of the AFE achieves 62.9 dB, and BPF based on a Small-Gm Operational Transconductance Amplifier (OTA) works in the frequency range of 0.5 Hz to 150 Hz. SAR-ADC achieve the ENOB of 7.5 with low power consumption and decent transition speed. The system with a total power consumption of 334.1uW will be supplied by Lithium-ion battery with a normal voltage at 3.7V, and the total input referred noise is 0.41uV. The fabrication process is AMI 0.6 um. All the schematic designs are simulated in Cadence Virtuoso, and the layout simulation is conducted in Cadence Layout.

Index Terms — Current balancing-IA, Small-Gm OTA, Low Dropout Regulator, SAR-ADC, ECG

I. INTRODUCTION

Cardiovascular disease (CVD) and Coronary heart disease (CHD) are two kinds of common heart diseases in recent years, all of which possess the ability to cause death directly. Usually, early detection of a disease could bring in-time treatment and effective prevention work. And it is estimated that almost 90% of CVD can be prevented as long as long-time monitoring and accurate diagnosis can be put into work [1]. Consequently, the awareness of health condition expedites the development of medical research significantly.

During each heartbeat, there exist tiny electrical changes on the signal, with addition of the fact that human body is conductive, meaning that a tiny amount of current will be generated and distributed among human skin. In other words, every time the heart beats, a pulse can be detected with respect to the time interval between two pulses and the amplitude of the signal due to the reason that heart always beats at a fixed frequency in normal condition. Therefore, the signal generated due to the heartbeat is called as electrocardiogram (ECG) signal [2]. Typical characteristics of ECG signal include low amplitude up to 1 mV and multiple kinds of noise [3]. Besides, ECG signal has a bandwidth of 0.5 Hz to 150 Hz [4], which can be captured by placing 12 electrode contacts on human body, for instance, left arm, right arm, right leg, etc. [5].

Wearable physiological monitoring systems have big advantages over traditional medical equipment because of their convenience and reliability. The signal will be sensed and captured by a sensor from patients, which means that when sensor is working, not only ECG can be detected, but also Electroencephalogram (EEG), skin temperature, and blood pressure, all of those signals are crucial parameters that could reflect and identify patient's physiology status [6]. A more accurate diagnosis could be obtained with more relevant parameters. With wearable devices, medical staff can monitor these important parameters while subject performs daily activities, with no necessity of staying in the hospital.

For the proposed system-on-chip in this paper, it is illustrated in Fig. 1. The signal is first sensed and collected by the sensor in the wearable physiological monitoring systems, and then fed into the input of Analog Front End (AFE) to be amplified. The small amplitude of ECG signal determines the requirement that the AFE is expected to have excellent performance in terms of high Common-Mode Rejection Ratio (CMRR) larger than 100 dB, high Power Supply Rejection Ratio (PSRR) no less than 60 dB, and low input referred noise lower than 10 uV RMS [7]. Due to interference in all frequency from surroundings, a filter should also be integrated to help researchers focus on signal in band of interest. Finishing the amplification process, the enlarged signal will flow into a SAR-ADC, which is to convert the analog signal collected into the digital code, because digital signal has the internal advantage of low rate of error when being transmitted by the off-chip transmitter and antenna. The transmitter in Fig. 1 can be implemented with the product, BN-ECG2, from BIOPAC Systems, Inc. [8].

![Diagram of system-on-chip](image-url)
In this paper, a system-on-chip is proposed for the application of ECG diagnostic, including an AFE and a SAR-ADC. In the first section, the background of ECG is introduced. In section II, based on theory, topology chosen for every block in the system is illustrated in detail. In the third section, simulation results are analyzed block by block. In section IV, state-of-art comparison is summarized and we present the work distribution for the design. At the end of the paper, conclusions and future work are addressed.

II. SYSTEM DESIGN

The system consists of reference circuit, instrumentation amplifier (IA), filter, amplifier stage and SAR-ADC, whose gain is expected to be greater than 60 dB. A reference circuit is used to generate and stabilize desired voltages and bias current for each branch of the whole system from 3.7V supply voltage. The ECG signal will first be collected from human body, and then fed into the input of IA to be scaled up 20 times afterwards. The output of IA will be connected with BPF so as to filter frequencies out of band of interest, 0.5 Hz to 150 Hz. The analog signal will flow into SAR-ADC after another amplifier stage with 45 dB gain.

A. Reference Circuit

The reference circuit can be separated into two parts: Beta-Multiplier Reference (BMR) and Low Drop-out Regulator (LDOR) [9][10].

BMR has two stable states: (1) initial state, the gate voltage of NMOS is zero and that of PMOS is supply voltage, there is no current in BMR; (2) normal state, the circuit functions properly, and is able to provide bias current for other blocks of the system. The topology used in this paper is BMR, which is presented in Fig. 2. The positive feedback loop formed by $M_1$, $M_3$ and the amplifier tend to latch the circuit state fast, and the negative feedback loop formed by $M_2$, $M_4$ will stabilize the reference voltage and bias current. If the circuit is at initial state, $M_5$ will be forced to turn on, meaning that current will be drawn from the gate of $M_3$ and $M_4$, the positive feedback makes sure that the circuit is switched to another stable state as soon as possible while the negative feedback stabilize the circuit. Two source-gate connected MOSFETs are used for coupling to reduce noise effect.

Aspect ratio of $M_2$ is set to be 6 times large as that of $M_1$, the voltage difference of $V_{GS}$ between $M_1$ and $M_2$ will be translated into a current determined by resistor $R$. The amplifier in the middle is a differential amplifier, the topology of which is shown in Fig. 3, with larger length, larger differential gain will be obtained, leading to the result that bias current is less sensitive to supply voltage change.

LDOR is used to generate supply voltage desired, VDD of 3.3V, from 3.7V battery voltage, $V_{bat}$. The topology of LDOR is presented in Fig. 4, voltage difference between $V_{ref}$ and $V_1$ is sensed, amplified by EA and fed into the gate of $M_1$. The negative feedback loop formed by EA, $M_1$ and $M_2$ will prevent $V_1$ from being affected by fluctuation of $V_{bat}$, moreover, $V_1$ will be forced to be same as $V_{ref}$. Transistors of $M_2$ and $M_3$ function as a voltage divider, which are implemented to generate VDD of 3.3V used in next stages from the stabilized voltage, $V_1$.

Error Amplifier (EA) in Fig. 4 is realized by a seven-transistor Operational Amplifier (OpAmp), shown in Fig. 5 [11]. The signal appearing at input will be amplified twice before it goes to output. A compensation capacitor and a zero-
nulling resistor are added to the OpAmp to prevent potential oscillation since the EA will be used in a feedback loop.

Fig. 4. Low Drop-out Regulator

B. Instrumentation Amplifier

Usually IA in the past is composed of three OpAmps and several matched resistors to achieve high CMRR, as shown in Fig. 6. It can be observed that there are seven resistors in this IA, the cost is either large area or significant amount of power since the IA will be integrated on chip, which makes this topology unsuitable for AFE for ECG application. Another drawback is its high power consumption consumed by three OpAmps. Besides, in order to achieve high CMRR greater than 100 dB, it requires the layout to be accurate to reduce mismatch since CMRR is directly related to the resistors in this topology.

In this paper, an IA using current-balancing technique is put into application, which consists of a transconducance stage and a transimpedance stage [12][13]. A simplified model of the IA is presented in Fig. 7, whose principle is the implementation of current feedback. The function of amplification is realized by amplifying the current converted from a voltage difference at input of IA, and reconverting the current to the output voltage.

Fig. 6. Classic IA

Fig. 7. Simplified model of current-balancing IA

In this paper, an IA using current-balancing technique is put into application, which consists of a transconducance stage and a transimpedance stage [12][13]. A simplified model of the IA is presented in Fig. 7, whose principle is the implementation of current feedback. The function of amplification is realized by amplifying the current converted from a voltage difference at input of IA, and reconverting the current to the output voltage.

Fig. 8 depicts the schematic of IA combined with a HPF, in which there exist a transconducance stage and a transimpedance stage. The IA is fully differential and in balance, a performance of high CMRR can be expected. Therefore, IA does not possess the functionality of amplification when there is no voltage difference across input. On the other hand, when IA is not in balance, the first stage will generate a current through a resistor $R_g$ from the input voltage across PMOS differential pair, the current is then mirrored to the next transimpedance stage which will translate the current to output voltage through the resistor $R_s$. The gain of IA can be expressed in (1) since the IA functions with the feedback.

$$A_{ad} = \frac{v_{out}}{v_{inp} - v_{bias}} = \frac{R_s}{R_g}$$

For ECG application, the CMRR must be larger than 90dB, and another requirement is to keep input referred noise less than $10 \mu V$ RMS since maximum amplitude of ECG signal is only 1mV. In this case, cascode current mirrors are implemented to reject common mode signal to boost CMRR.

The input transistors of IA are selected to be PMOS differential pair for the reason that PMOS are less noisy when compared with NMOS. Because the frequency range of ECG signal is from 0.5 Hz to 150 Hz, flicker noise is the dominate interference to the ECG signal as shown in Fig. 9 [14].
The input referred noise and thermal noise of a transistor fabricated by standard CMOS process can be expressed in (2) and (3), respectively.

\[
\overline{V}_{n,\text{in(flicker)}}^2 = \frac{K_x}{C_{ox}(W/L)^x} \frac{1}{f} \tag{2}
\]

\[
\overline{V}_{n,\text{in(thermal)}}^2 = 4KTR \cdot \frac{2}{3g_{m,\text{inp}}} \tag{3}
\]

Based on (2) and (3), the size of transistors \( M_1 \) - \( M_4 \) should be large to reduce input referred flicker noise and thermal noise.

In order to focus on signal within the band of interest, a LPF is integrated with IA. Capacitor \( C \) is placed in parallel with resistor \( R \) to form a low pass filter to reject signal with frequency larger than 150 Hz, such that the 3 dB cutoff frequency can be derived from (4).

\[
f_{\text{LPF}} = \frac{1}{2\pi RC} \tag{4}
\]

The IA is implemented in a feedback loop, compensation capacitor \( C \) and zero-nulling resistor \( R \) should be added when taking stability into account.

C. Band-Pass Filter

For ECG application, the amplitude of signal is small, meaning that DC offset can be destructive if it exceeds 0.1 mV, DC signal should be eliminated as a result. The HPF can be a good solution to cancel low frequency noise as well as eliminate DC offset at the same time.

In this paper, Gm-C filter is applied since it can yield a large resistance without too much area cost, and it is integrated in the feedback loop of IA as is shown in Fig. 8. Signal from output will flow into a LPF formed by an Operational Transconductance Amplifier (OTA) so that only low frequency signal will pass and flow into the another input of the Transimpedance stage of IA. An equivalent effect of a HPF will be produced because the input of the transimpedance stage is a PMOS differential pair whose function is to subtract two signals at the input, reject low frequency signal in common.

Therefore, we will call this equivalent HPF produced by LPF and IA as HPF. After the integrated LPF in IA, high frequency signal will also be filtered as a result, meaning that an equivalent BPF can be obtained.

A typical Gm-C filter is shown in Fig. 10, whose cutoff frequency can be derived through (5) [15].

\[
f_{\text{HPF}} = \frac{G_m}{2\pi C_{\text{filter}}} \tag{5}
\]

Gm-C filter is implemented as shown in Figure 10. The drawback of this topology is the necessity of using a large \( C_{\text{filter}} \), and thus it will still occupy large space.

![Typical Gm-C filter](image)

An alternative way of design is the application of Small-Gm OTA, the capacitor used for filtering can be reduced due to small transconductance of OTA [16]. The schematic diagram of HPF based on Small-Gm OTA is presented in Fig. 11.

![Small-Gm filter](image)

In Fig. 11, top PMOS transistors set bias current in each branch, and bottom NMOS transistors consist of a current mirror. The principle idea of this HPF is current division. By setting the size of \( M_{11} \) and \( M_{21} \) to be M times larger than
that of $M_{12}$ and $M_{22}$ respectively, the current in the branch of $M_{12}$ and $M_{22}$ will be $M+1$ times of the bias current set by PMOS transistors. And voltage difference between $V_{bias}$ and $V_{out}$ will be converted into current flowing into $M_{g1}$ and $M_{g2}$. We are able to bias $M_{g1}$ and $M_{g2}$ in triode region through tuning the aspect ratio of $M_{c}$. The overall $Gm$ is expressed in (6).

\[
G_m = \frac{g_{M_{g}}}{M + 1}
\]  

Fig. 8. Schematic of proposed current-balancing IA with BPF

M is the aspect ratio of $M_{12}$ to $M_{12}$. $g_{M_{g}}$ is the conductance of $M_{g1}$ and $M_{g2}$. The HPF is designed to achieve a 0.5 Hz cutoff frequency.

D. Amplifier Stage

A second gain stage is designed in order to further amplify the signal collected. And before the signal going into ADC, there exists a buffer between the output of IA and the input of ADC to avoid delay since the input of capacitance of SAR ADC is relatively large.

A common source amplifier is selected as the second gain stage to extend the signal swing to almost rail-to-rail, therefore, a buffer with rail-to-rail Input Common Mode Range (ICMR) and large output swing is expected after the second gain stage. The schematic of whole stage is presented in Fig. 12.

The NMOS on the bottom of common source amplifier is biased in triode region to shift the output voltage to half VDD, 1.65 V. The NMOS and PMOS differential pair make it possible that beyond rail-to-rail ICMR can be satisfied, and a high open loop gain can be determined by folded cascade structure. Besides, no compensation capacitor needs to be applied due to the simplicity of the circuit.
E. ADC Design

Low power ADC with moderate resolution and low sampling frequency is quite suitable for biomedical application. For those reasons, SAR-ADC is one of most popular topology to be used in biomedical field. SAR-ADCs also have low power consumption and good ability on size scaling due to its large amount of digital components. In this project, we designed a 8-bit ADC and implemented with AMI 0.5um technology with low power and accurate resolution.

1) Successive Approximation algorithm

SAR-ADC employed a binary search algorithm and go through bit by bit. It starts with the MSB setting to 1, if the output voltage of D/A is higher than Vref/2, the MSB will remain 1, and next bit will be set to 1 and compared to 3Vref/4, then 7Vref/8, 15Vref/16, etc. However, if output voltage is lower than Vref/2, MSB will be switched to 0. In either case, the value of MSB is determined and the algorithm goes to the next bit and repeat the same steps until all the bits are determined.

2) Charge Redistribution Architecture

This topology implements a capacitive DAC which also operates as a sample and hold circuit. The block diagram of this DAC is illustrated in Fig. 14. The DAC usually contains a binary weighted capacitor array. During each conversion, the analog input is first sampled and stored in the capacitor array, then the output of the DAC is compared with Vcm for N clock cycles to generate digital output, the output voltage of DAC will gradually follow and reach to Vcm at the end of each conversion.

3) Design implementation

Fig. 15 illustrates our ADC design schematic and figure 15 is floor plan of our ADC after layout.

The first breakdown of our design is the sample and hold circuit. To ensure high conversion speed and avoid too much KT/C thermal noise in our DAC, we chose the smallest capacitor value to be 20 fF. During the sample period, the top switch is on and the DAC samples analog input signal into the capacitor array. During the hold period, the sample signal is low and top switch turns off and bottom switch change to Vref and comparison starts. One thing worth notice is the leakage current from the top switch could be significant and thus negatively affects the linearity of the DAC, [17] to alleviate this problem, a two-pmos topology is used for better gating current.
Table 1 shows the operation condition of the bottom plate switch.

```
<table>
<thead>
<tr>
<th>Sample</th>
<th>Digital Data</th>
<th>Bottom plate voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>x</td>
<td>Vin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Vref</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>gnd</td>
</tr>
</tbody>
</table>
```

The next breakdown is SAR control logic. The SAR we designed is a combination of a ring counter and a code register.

All registers are designed using master-slave flip-flops. Each conversion needs at least 10 clock cycles. During first cycle, the registers are reset and all outputs are zero. Next 8 cycles the counter will pass a one from MSB to LSB, the last cycle is for register to complete conversion and output the digital data. Fig. 20 shows the master-slave flip-flop design and Fig. 21 and 22 shows the complete SAR.

Comparator is a very important component in ADC design. For low power applications, dynamic latched comparators are favored over static latched ones. For our project, we use a power efficient two-stage latch comparator which is fast and has low input referred offset voltage.
Fig. 23. Two-stage dynamic latch comparator design.

The top stage is a voltage amplifier and the bottom stage is a latch. In the reset stage where the clock is low, Q1 and Q3 charge two stage-connecting nodes to Vdd and output is zero because latch is off. When clock turns to high, tail transistor is on and amplification starts, the two stage-connecting nodes drop voltage differently due to the input voltage difference, and with the help of positive feedback, the output turns to high.

Figure 24. Comparator layout.

III. PERFORMANCE AND SIMULATION RESULTS

All the schematic simulations are conducted in Cadence Virtuoso, and the layout is simulated in Cadence Layout. The fabrication process is AMI-0.5 um.

A. Full Analog Front End

The CMRR of current-balancing IA with an integrated LPF is demonstrated in Fig. 25, the minimum CMRR exists at 150 Hz, which is 132.87 dB. For the full AFE, from IA to amplifier stage, the frequency response is shown in Fig. 26. It can be observed that -3 dB gain is 59.9 dB while the maximum can reach 62.9 dB when the frequency range is from 0.495 Hz to 154 Hz. Total input referred noise accomplishes 0.41 μV RMS, which is far below the specification. Apart from that, the ICMR of AFE is 0.4 V to 1.777 V, output swing is 0.23 V to 3 V. The positive PSRR is greater than 95 dB, and the negative PSRR is no less than 67.35 dB. All the specifications are summarized in Table I and compared with state-of-art designs, which will be illustrated in the next section.

B. SAR ADC

Our ADC operates under 1kHz clock frequency and 3.3 V power supply, the sampling rate is 400 S/s and overall power consumption is 5.8μW. Table 2 shows the power breakdown of the ADC.

The comparator has a propagation delay of 1.4 ns and input-referred offset of 8.1 mV. We implemented unity feedback reset switch to the comparator for offset cancellation.

Fig. 29 shows the transient response of digital output data of SAR, notice the bit shift start with the second cycle after reset turns low, and end with the ninth clock cycle.
Table 2. Power breakdown for ADC

<table>
<thead>
<tr>
<th>Component</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC</td>
<td>3.43uW</td>
</tr>
<tr>
<td>SAR</td>
<td>1.39uW</td>
</tr>
<tr>
<td>Comparator</td>
<td>0.9uW</td>
</tr>
<tr>
<td>Clock</td>
<td>64.7nW</td>
</tr>
<tr>
<td>Total</td>
<td>5.8uW</td>
</tr>
</tbody>
</table>

We detected input referred noise to be about 15mV, thus our calculated SNR is

$$\text{SNR} = 20 \log_{10}(\frac{V_{dd}}{V_{\text{noise}}}) = 46.85 \text{ dB}$$

We also know that

$$SNR = 20 \log_{10} \left( \frac{2N_{\text{LSB}}}{\sqrt{2} \cdot V_{\text{LSB}} \cdot \sqrt{12}} \right) = 6.02N + 1.76$$

Thus, our ENOB is SNR-1.76 / 6.02 = 7.5

IV. STATE-OF-ART COMPARISON AND WORK DISTRIBUTION

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>3.7</td>
<td>1.8</td>
<td>3.3</td>
</tr>
<tr>
<td>Process Technology (um)</td>
<td>AMI 0.6</td>
<td>0.18</td>
<td>0.18</td>
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<tr>
<td>Gain of AFE (dB)</td>
<td>62.9</td>
<td>45</td>
<td>N/A</td>
</tr>
<tr>
<td>Power consumption (uW)</td>
<td>241.8</td>
<td>138</td>
<td>132</td>
</tr>
<tr>
<td>Total Input referred noise</td>
<td>0.41</td>
<td>0.278</td>
<td>2.3</td>
</tr>
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<td>----------</td>
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<td></td>
</tr>
<tr>
<td>(RMS)(uV)</td>
<td>132.87</td>
<td>127</td>
<td></td>
</tr>
<tr>
<td></td>
<td>122</td>
<td></td>
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</tr>
<tr>
<td>CMRR (dB)</td>
<td>95</td>
<td>65</td>
<td></td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td></td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>Frequency Range (Hz)</td>
<td>0.495 - 154</td>
<td>0.2 - 200</td>
<td>0.05 - 125</td>
</tr>
<tr>
<td>ICMR(V)</td>
<td>0.4 - 1.78</td>
<td>0.45 - 1</td>
<td>0 - 1.65</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>TABLE II. WORK DISTRIBUTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Member</td>
</tr>
<tr>
<td>Yang Xu</td>
</tr>
<tr>
<td>Yanling Wu</td>
</tr>
<tr>
<td>Xiaotong Jia</td>
</tr>
</tbody>
</table>

V. CONCLUSION

In this paper, a system-on-chip for ECG diagnostic is proposed, including AFE and SAR-ADC. Total power consumption achieves 334.1uW, with AFE and SAR ADC included. The gain of AFE is 62.9 dB while current balancing IA demonstrates greater than 132 dB CMRR within the band of interest. The frequency range of Gm-C filter is from 0.5 Hz to 150 Hz. For AFE, we implemented a 8-bit ADC with ENOB of 7.5 bit and power consumption of 5.8uW which is very low. We also realized there is an important tradeoff when designing the DAC, with higher speed, the noise will increase and affect many key performance of our AFE, such as linearity and distortion. For AFE, future work will be dedicated to further reduce transconductance for BPF to decrease capacitor for filtering, and implementing Driven Right Leg Circuit to reject interference and noise; For SAR ADC, further noise reduction method needs to be exploited to achieve better performance while still maintain low energy and high speed.

REFERENCES


