An 8-Channel General-Purpose Analog Front-End for Biopotential Signal Measurement

Xue Yang, Jinming Hu, Zengweijie Chen, Hang Yang

Abstract—This paper presents system level specifications of an 8-channel CMOS analog front-end (AFE) with an 11-bit analog to digital converter, which is used for acquiring certain biopotential signals such as EEG, ECoG, ECG, and EMG, i.e. signals for brain activities, heart activities, and muscle activities.

I. INTRODUCTION

Biopotentials are electrical signals; they are generated due to action potentials produced from certain type of cells which are components of nerve, muscle, or heart tissues. Among all kinds of biopotentials, the most common ones are EEG, ECoG, ECG, and EMG. EEG and ECoG are introduced by brain cells; ECG is generated by the heart; and EMG is from the muscle activity [1]. As a result, the signals are of great value in obtaining information about structure and function of particular tissues from which they are generated from. However, these medical benefits largely depend on the accurate acquisition of the electrical signals. In addition, with growing number of the global aging population, demand for health monitoring devices has never been higher. Hospitals have invested substantial resources and capital to track various kinds of biopotential signals for each individual, because each type of electrical signals requires different kinds of medical equipments. Thus, it is a logical choice to build a general-purpose and accurate analog front-end for a biopotential signal recording system.

The AFE presented in this paper will be used to record EEG, ECoG, ECG and EMG signals whose amplitudes range from 5μV to 5mV and bandwidths range from dc to 2 kHz as shown in Table 1 [1]. Thus the system must introduce very little noise, have a high common-mode rejection ratio (CMRR), and have a high power supply rejection ratio (PSRR). Regarding the extremely low range of target signals, a lowpass filter with 2 kHz will be developed. As biopotential signals are collected through physical electrodes, the input of the system must have huge input resistance to minimize loading effect. Moreover, the differential DC offset created by tissue-electrode interface should also be eliminated to avoid output saturation. It is done by a chopper low noise amplifier (LNA).

According to Table 1, the smallest amplitude of the four signals is 5μV and the common bandwidth is around from 0.01Hz to 2kHz. Consequently, the bandwidth of the whole system is from 0.01Hz to 2kHz. An analog to digital converter (ADC) has a step size granularity of 5μV (before amplification) is chosen to be 11 bits (2048 steps).

<table>
<thead>
<tr>
<th>Biopotential Signal</th>
<th>Amplitude (μV)</th>
<th>Bandwidth(Hz)</th>
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<tbody>
<tr>
<td>EEG</td>
<td>0.005 - 0.3</td>
<td>0.5 - 150</td>
</tr>
<tr>
<td>ECoG</td>
<td>0.01 - 3.5</td>
<td>0.5 - 500</td>
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<tr>
<td>ECG</td>
<td>0.5 - 4.5</td>
<td>0.01 - 250</td>
</tr>
<tr>
<td>EMG</td>
<td>0.1 - 5</td>
<td>dc - 2kHz</td>
</tr>
</tbody>
</table>

Fig. 1. System block diagram

II. SYSTEM

The block diagram of the proposed system is given in Figure 1 and the system level specifications are summarized in Table 2. This section will address each of the blocks individually.
A. Pre-Amplifier

For our circuit, a preamplifier stage is used for the purposes of amplifying extremely low amplitude neural signals provided as input, with minimal noise and/or interference. Chopper stabilization is used with a chopper amplifier, which is a technique that modulates and amplifies a desired signal at a higher frequency to reduce noise, then demodulates back to baseband. Flicker noise and offset voltage of the amplifier are shifted to a chopping frequency, where they can then be eliminated using a low-pass filter [1].

![Fig. 2. Telescopic OTA design [2].](image)

An OTA shall be chosen as the chopper amplifier with telescopic structure for low power consumption and low noise (topology shown in Figure 2 above). Input devices may also be chosen as PMOS due to significantly less flicker noise than their NMOS counterparts [2].

B. Programmable Gain Amplifier

PGA is the final stage of the AFE. It accepts signals of various strengths from the previous stage, and will scale to match the maximum ADC input [4], and hence ensure the quality of ADC output. The PGA’s gain can be conveniently changed via $f_{\text{clock}}$ and variable capacitors. The sampling rate, $f_{\text{clock}}$, is set to the same as the analog multiplexer’s at 500k channels/s. The device is built via using a capacitive-reset gain typology. A famous circuit, differential-to-single-ended gain circuit using capacitive-reset typology, is utilized in this paper (see Fig. 3). Correlated double sampling (CDS) technique is also being applied in Fig. 3 to minimize errors from offset voltages and $\frac{1}{f}$ flicker noise [3].

![Fig. 3. A differential-to-single-ended gain circuit using capacitive reset [3].](image)

With C1 being as the variable capacitor, the gain of the switched capacitor circuit is $C1/C2$.

C. Clock Signal Generation and Distribution

An exterior oscillator will be used to provide clock signals, which makes certain components to be effective. The frequency of the clock signal is 1 MHz, and a set of on-board clock divider will provide proper clock frequencies in accordance to modules’ needs. Maxim MAX7375AXR105+T is a good candidate for our application, which is available in the market for $0.73/unit. The rise time/slew rate will be monitored during validation stage.

D. Analog 8-1 Multiplexer

The multiplexer module is comprised of a CMOS switching array, a switch control unit, and differential difference amplifier serves as a buffer. The switching rate of the switches is set to 500k channels/s. Hence, a clock signal of 500kHz is needed for such module [1][5].

![Fig. 4. Implementation of Multiplexer via a Differential Difference Amplifier](image)

E. ADC

Since the smallest amplitude of the four signals is 5μV and the common bandwidth is around from 0.01 Hz to 2 kHz, the ADC should have a step size granularity of 5μV (before amplification) and its speed can be relatively slow. Thus, the 11 bits Successive Approximation data converter topology is chosen due to its medium speed, low cost and decent resolution [6]. The sampling rate of it is chosen to be 6k, which is 3X of the Nyquist frequency.
III. TASKS AND DIVISION OF LABOR

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<table>
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<tbody>
<tr>
<td>Jinming Hu</td>
<td>Pre-Amplifier, Programmable LPF</td>
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<tr>
<td>Xue Yang</td>
<td>PGA, ADC</td>
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<td>Zengweijie</td>
<td>Clock, ADC, Analog Multiplexer</td>
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<td>Chen</td>
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<td>Hang Yang</td>
<td>Bandgap Reference, Voltage Generator</td>
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</tbody>
</table>

References


Side-note: in order to properly scale our block diagram, we broke the 2-page limit on putting the essential information (a little bit).