A CMOS-Based SoC for Luminescence Monitoring of Glucose Metabolism

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Abstract—In this manuscript, we propose a luminescence system-on-a-chip (SoC) for glucose metabolism in neural tissue to monitor patient stroke recovery. To provide a more holistic depiction of glucose metabolism, both glucose and oxygen are monitored via luminescence probes whose emission signals are filtered optically and absorbed via photodiodes. The photodiode output current is typically small in magnitude, on the order of nA. In order to amplify this current to reasonable levels for signal processing, an analog front-end and data converter are required. For the analog front end, we propose a high gain, low noise, and low offset transimpedance amplifier to bring the small current to a reasonable voltage. This voltage can be sampled and then converted to a digital signal using a Σ∆-analog to digital converter. Finally, using a wireless transmitter block operating in the ISM band we can sent out the Σ∆-modulated data to be processed externally through software.

Index Terms—luminescence, glucose metabolism, oxygen, photodiode, ADC, TIA, switched-capacitor circuits

I. INTRODUCTION

Stroke affects nearly 800,000 Americans per year, resulting in nearly 130,000 fatalities [1]. Of all of the strokes that have proven fatal, over 80% of these strokes are ischemic, implying that blood flow to the brain has been hindered [1]. Therefore, to ensure appropriate recovery after a stroke has been detected and surgery has been conducted, the blood flow of the brain needs to be monitored as post-surgery treatment is administered. Studies have demonstrated a correlation between cerebral blood flow and glucose metabolic rate [2]. Therefore, an implantable device that can measure glucose metabolism of neural tissue can prove useful for helping monitor stroke recovery.

Glucose metabolism has been well-characterized in mammalian cells and is the generation of biochemical energy as adenosine triphosphate (ATP) using glucose and oxygen as reactants. Measuring these reactants can therefore provide a metabolic footprint describing the overall health of the brain.

For several decades, numerous biomedical assays have used luminescent light intensity to measure biomolecular concentrations [3]. Studies have demonstrated that fluorescent probes used for glucose measurements can be embedded into implantable microbeads or integrated into a catheter [4]; in fact, a CMOS-based implantable glucose biosensor that uses an anthracene-based dye embedded within a hydrogel has already been manufactured and tested in rats [5]. Implantable palladium porphyrin-based oxygen phosphorescent indicator dyes are also available to quantify relative oxygen levels. These dyes have been packaged in devices that have been implanted into rats and thus prove promising as indicator dyes for an implantable oxygen sensor [6].

In light of the aforementioned motivations, we propose an implantable CMOS-based luminescence sensing system-on-chip (SoC) designed to quantify glucose and in-tissue oxygen levels. Section II describes the system architecture and delves into the design specifications and more detailed architecture for each block. The manuscript ends with a table of the work distribution among team members for this project.

A. Biological Design Specifications

Since this project encompasses designing a CMOS-based biosensor for luminescence signal detection, we need to ensure that the minimum current detection limit corresponds to an appropriate luminescence signal for both in-tissue oxygen and glucose. For glucose fluorescent sensing, the maximum detectable current should be 7.2 nA assuming an incident optical power of 1 µW, assuming that 100% of the photons emitted are absorbed, noting a quantum efficiency of 8% as presented in the literature [7], [8], and using a photodiode with the optical filter in [9] to provide 90% transmission and 0.1 A/W of incident optical power [10]. In the case of oxygen biosensing, the maximum detectable current should be 1.8 nA assuming an incident optical power of 0.1 µW, 100% photon absorption, a quantum yield of 5-10% as demonstrated in the literature [6], an optical filter with 90% transmission [11] and a responsivity of 0.2 A/W of incident optical power based on the photodiode in [12]. To provide sufficient field of view as well as reasonable current generation for a low incident optical power, the photodiodes can be off-chip and connected to different input pads of our SoC (Figure 1). The optical excitation sources for glucose and oxygen sensing will be a laser of wavelength 400 nm pulsed at a kHz-frequency. This design choice is to ensure that the time course of glucose metabolism can be appropriately monitored and that both luminescent probes can be excited using the same excitation source. To avoid issues of light scattering from the fluorescing sample, a fully differential topology starting from the input is

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avoided, and a SE-to-FD converter is used instead. Additionally, the size of the system should be no more than 1 cm² (excluding the excitation source, which can be generated from an LED and corresponding control circuit as a separate SoC that can be implanted appropriately using a catheter and appropriate surgical instrument).

B. Prior Work

Prior work in luminescent sensors has focused on using on-chip photodiode arrays to perform fluorescent imaging. In [13] the circuit design sought to maximize the sensor dynamic range and minimize the overall input referred noise of the circuit. In this architecture they use current-mode sampling and a differential ADC to directly sample the current from each pixel in their photodiode array. In [14], for a similar imaging application, a chopping amplifier style architecture was utilized. A chopping amplifier topology minimizes the effect of amplifier offset voltage and avoids dominant 1/f noise from the active devices. Both works use differential topologies to reject common-mode noise. In [15], an analysis of noise contribution for the analog front-end has shown that the primary noise contributors are the photodiode current, transimpedance amplifier noise, and switching noise in the switch capacitor circuit. Based on this, to improve SNR at the output, the noise contribution from the transimpedance amplifier and sample and hold should be minimized. Based on these characteristics and the circuit architectures presented in [13] and [14], we present our proposed system architecture composed of a transimpedance amplifier (TIA), sample-and-hold circuit, 2:1 multiplexer to toggle between glucose and oxygen sensing inputs, a single-ended to fully-differential converter, an ADC, and a wireless transmitter. The portion boxed in yellow designates what will be designed for the course (Fig. 1).

II. SOC SYSTEM ARCHITECTURE

A. Transimpedance Amplifier

Since the photodiodes will provide a small current, adequate amplification is required to bring it to a usable range for signal processing. As the first amplifier in the overall system, the noise from this stage determines the overall sensitivity of the entire chip. Transimpedance amplifiers (TIA) have been shown to provide high gain and low noise that is suitable for biomedical applications (see [16]-[19]). In a TIA, transimpedance gain on the order of MΩ has been reported in [16]-[19]. However, there exists a tradeoff between the gain and bandwidth of the amplifier. In addition, low noise techniques such as correlated double sampling (CDS) ([18]) and chopping ([14]) are commonly used. To reduce the bandwidth requirement, integrator-based TIAs have been designed for high gain in [16]. Table I defines state of the art performance and our specifications for the TIA.

Since we are interested in not only the DC characteristic of the photodiode response, we choose not to use a chopping amplifier topology. Using an ideal operational amplifier, the schematic and preliminary simulation results are shown in figures 2 and 3, respectively. Here we look at the AC response of the TIA to show the 140dB transimpedance gain and bandwidth specification. Noise is also shown but since the operational amplifier is ideal, this is only the noise of the switched capacitor elements. Figure 4 shows the transient integrator behavior of the switched capacitor TIA.

![Figure 1. System-level diagram of luminescence-based SoC.](image1)

![Figure 2. Schematic of TIA assuming ideal op amp.](image2)

![Figure 3. AC response for TIA.](image3)

![Table I: State-of-the-Art Performance for TIA](table1)
B. Sample and Hold

Upon receiving the voltage output from the TIA, the circuit must store this output so that it can eventually be converted to a digital value by the analog-to-digital converter (ADC). A sample-and-hold circuit can be used to successfully capture and store this output on a capacitor. Upon choosing a sample-and-hold topology, maintaining minimal layout area, minimum noise, and the value of the voltage output are critical considerations. Therefore, the topology should implement the minimum number of switches and capacitors while avoiding charge injection, clock feedthrough, and instability.

In light of the aforementioned design considerations, a simple sample-and-hold circuit with a pass gate for a switch is chosen and simulated with a unity gain buffer to avoid loading the subsequent stage (Figure 5). Since we are at the stage of system-level and behavioral simulations, an ideal op amp was assumed. The pass gate minimizes charge injection by forcing an approximately equal proportion of electrons and holes to be injected into its source and drain nodes upon switching. The aspect ratios of the transistors were chosen so as to minimize charge leakage during the hold period while maintaining appropriate circuit bandwidth. Simulation results of the sample-and-hold circuit assuming a 2 pF load capacitance are presented in Figure 6. We note that the output appropriately tracks the input. A square wave simulation was also run to more realistically emulate a pulsed laser source of 1 kHz frequency, and the output successfully tracked the input within 1 ms.

C. 2:1 Multiplexer and Single-Ended to Fully Differential Converter

Since both glucose and oxygen need to be monitored, a multiplexer is required to switch between inputs. To accomplish this goal, we use a 2-to-1 mux using transmission gates. Transmission gates allow us to pass both high and low voltage signals. The schematic of this circuit can be seen in figure 7. The corresponding simulation result can be seen in figure 8. In this simulation the mux initially selects the square wave input and then switches to the sinusoidal wave input when the select signal fall (red curve).

The single-ended to fully differential converter (Figure 9) will take the output of the multiplexer and provide a differential input to the ADC. This will be accomplished using a switched
capacitor circuit as seen in [20]. Unlike the low frequency clock for the TIA and sample and hold circuit, this switched capacitor circuit will operate off of the same high speed clock as the ADC. Figure 10 depicts a preliminary simulation with a 200mV amplitude sinusoidal signal as the input. Here it can be seen that the single-ended input (top pink signal) produces two fully out-of-phase differential output sinusoidal signals (orange and green). The amplitude of the sinusoidal signal is a reasonable expectation of the expected input to the SE-to-FD converter, considering the input current and gain that can be expected at this point in the system.

D. Clock Generation

Since we are using wireless power transfer to power the device we can use the power clock as the master clock of our system. This clock operates at 13.56 MHz. Based off of this clock all subsequent clocks are the result of frequency division. For the TIA we generate a 3.31 kHz clock which corresponds to a division factor of 4096 from the master clock. To generate these division ratios, we will be using a chain of 12 D flip-flops. The flip-flops are created using transmission gates and inverters. An advantage of this for our system level design is that all intermediate clocks are available if we choose to use a high or lower set of frequencies for the switched capacitor clocks. Once the clock frequency is correctly selected, digital logic can be used to generate non-overlapping clocks suitable for switched capacitor circuits. A schematic of this can be shown in figure 11. By sizing the inverters for larger delay the non-overlapping time can be adjusted for system level constraints. Figure 12 shows non-overlapping clocks (bottom green and orange) with a frequency divided clock of 3.31 kHz.

Figure 9. Schematic of SE-to-FD conversion.

Figure 10. Simulation demonstrating SE-to-FD conversion.

Figure 11. Schematic of clock generation.

Figure 12. Simulations demonstrating non-overlapping clock generation.
E. Bias Generation

For low-power analog systems, a low bias current reference is preferred. In addition, for an implantable solution, the bias current should have minimum temperature dependence around average human body temperature (37°C). For this reason, the bias generator (Figure 13) was designed with low current and low temperature dependence. To accomplish this objective, the sizing of the transistors in the beta multiplier is scaled down. Additionally, since temperature dependence is a function of the biasing resistor, it is possible to design the current and temperature dependence at the same time. The results of this are shown in Figure 14. Here a 355nA current is shown. This current can be mirrored to generate approximately 1µA with a current mirror aspect ratio of 3. The temperature dependence shows zero crossing for temperature dependence around 37°C which corresponds to human body temperature.

F. First-Order Switched Capacitor ΣΔ-ADC

Once the signal has been captured and amplified by the analog front-end, the voltage representation of the fluorescence signal will be digitized and sent to the communication block of our SoC. The most commonly utilized ADC types in industry and academia are the flash, dual slope, successive approximation (SAR), pipeline, and ΣΔ ADCs. After considering trade-offs between complexity, power consumption, speed, resolution, and size, we will implement a 1st order switched capacitor ΣΔ ADC with differential inputs. This type of ADC achieves a very high resolution and low power at the expense of speed. Our system will operate in an open-loop configuration and, therefore, speed is not a stringent requirement in our design. In addition, the data acquisition will not be processed in real-time, therefore, the delay introduced by the ΣΔ ADC will not reduce the overall performance of the entire system.

For the SoC, minimizing power consumption while increasing bit resolution is of extreme importance since the fluorescence signal could be on the order of picoamperes, and the entire system will be power limited. One of the advantages of ΣΔ converters is that they perform the function of noise shaping by moving the low frequency noise to high frequencies outside the bandwidth of interest, thus allowing for the acquisition of very low frequency signals with a high degree of accuracy. We estimate that a 9-bit resolution for our ADC will give us enough accuracy from 20pA to 10nA to detect changes in the fluorescence of 1 part in 500.

Figure 15 shows the system level diagram of the switch capacitor ΣΔ converter. The switch capacitor ΣΔ converter is implemented using a fully-differential trans-conductance stage.
amplifier to perform the integration, a switch capacitor based subtraction of the digital-to-analog converter output (DAC) and the analog input coming from the single ended to fully differential block, a comparator, a flip-flop, and a simple switch capacitor DAC. The \( \Sigma \Delta \) converter is oversampled at 1MHz, which is equivalent to a minimum oversampling rate of 250. Based on simulations using ideal components and switches, an equivalent number of bits of 9 was obtained while using an input voltage signal of 500mV, which is equivalent to a minimum detectable signal of 1mV or 300fA. Figure 16 shows the frequency spectrum of the \( \Sigma \Delta \) converter. Additionally, the sensing current range of the entire system can be changed by adjusting the reference voltages of the \( \Sigma \Delta \) converter and the gain of the input trans-impedance amplifier, which allows for a system with a more flexible input current range.

G. Wireless Transmission Link

To build the full SoC beyond the scope of ECE6414 a wireless transmitter is required. For data transfer, we envision a wireless transmission link operating in the ISM band at 915MHz. The transmitter block will consist of a Tristate Class-D amplifier driving a surface mounted antenna (Johanson Technology). The Class-D amplifier will be driven by a voltage controlled oscillator (VCO) implemented with a closed loop phase-locked loop (PLL) for frequency stability, as a result, our system will not need off-chip components for the wireless link.

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>POWER BUDGET</th>
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</thead>
<tbody>
<tr>
<td>Circuit Block</td>
<td>Power Budget</td>
</tr>
<tr>
<td>TIA</td>
<td>3 mW</td>
</tr>
<tr>
<td>Sample-and-Hold</td>
<td>0.5 mW</td>
</tr>
<tr>
<td>SE-to-FD Converter</td>
<td>1 mW</td>
</tr>
<tr>
<td>Clock Generation</td>
<td>2 mW</td>
</tr>
<tr>
<td>Multiplexer</td>
<td>1 mW</td>
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<tr>
<td>ADC</td>
<td>5 mW</td>
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<tr>
<td>Wireless Link</td>
<td>30 mW</td>
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<tr>
<td>Bias Generator</td>
<td>0.1 mW</td>
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<tr>
<td>Total Power</td>
<td>42.6 mW</td>
</tr>
</tbody>
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The closed-loop PLL implementation will also result in a more robust wireless link.

REFERENCES
