A CMOS-Based SoC for Luminescence Monitoring of Glucose Metabolism

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I. INTRODUCTION AND MOTIVATION

Stroke affects nearly 800,000 Americans per year, resulting in nearly 130,000 fatalities [1]. Of all of the strokes that have proven fatal, over 80% of these strokes are ischemic, implying that blood flow to the brain has been hindered [1]. Therefore, to ensure appropriate recovery after a stroke has been detected and surgery has been conducted, the blood flow of the brain needs to be monitored as post-surgery treatment is administered. Studies have demonstrated a correlation between cerebral blood flow and glucose metabolic rate [2]. Therefore, an implantable device that can measure glucose metabolism of neural tissue can prove useful for helping monitor stroke recovery.

Glucose metabolism has been well-characterized in mammalian cells and is the generation of biochemical energy as adenosine triphosphate (ATP) using glucose and oxygen as reactants. Measuring these reactants can therefore provide a metabolic footprint describing the overall health of the brain.

For several decades, numerous biomedical assays have used luminescent light intensity to measure biomolecular concentrations [3]. Studies have demonstrated that fluorescent probes used for glucose measurements can be embedded into implantable microbeads or integrated into a catheter [4]; in fact, a CMOS-based implantable glucose biosensor that uses an anthracene-based dye embedded within a hydrogel has already been manufactured and tested in rats [5]. Implantable platinum porphyrin-based oxygen phosphorescent indicator dyes are also available to quantify relative oxygen levels. These dyes have been packaged in devices that have been implanted into rats and thus prove promising as indicator dyes for an implantable oxygen sensor [6].

In light of the aforementioned motivations, we propose an implantable CMOS-based luminescence sensing system-on-chip (SoC) designed to quantify glucose and in-tissue oxygen levels. Section II describes the system architecture and delves into the design specifications and more detailed architecture for each block. The manuscript ends with a table of the work distribution among team members for this project.

A. Biological Design Specifications

Since this project encompasses designing a CMOS-based biosensor for luminescence signal detection, we need to ensure that the minimum current detection limit corresponds to an appropriate luminescence signal for both in-tissue oxygen and glucose. For glucose fluorescent sensing, the maximum detectable current should be 7.2 nA assuming an incident optical power of 1 µW, assuming that 100% of the photons emitted are absorbed, noting a quantum efficiency of 8% as presented in the literature [7], [8], and using a photodiode with the optical filter in [9] to provide 90% transmission and 0.1 A/W of incident optical power [10]. In the case of oxygen biosensing, the maximum detectable current should be 4.5 nA assuming an incident optical power of 0.1µW, 100% photon absorption, a quantum yield of 10-25% as demonstrated in the literature [6], an optical filter with 90% transmission [11] and a responsivity of 0.2 A/W of incident optical power based on the photodiode in [12]. To provide sufficient field of view as well as reasonable current generation for a low incident optical power, the photodiodes can be off-chip and connected to different input pads of our SoC (Figure 1).

B. Prior Work

Prior work in luminescent sensors has focused on using on-chip photodiode arrays to perform fluorescent imaging. In [13] the circuit design sought to maximize the sensor dynamic range and minimize the overall input referred noise of the circuit. In this architecture they use current mode sampling and a differential ADC to directly sample the current from each pixel in their photodiode array. In [14], for a similar imaging application, a chopping amplifier style architecture was utilized. A chopping amplifier topology minimizes the effect of amplifier offset voltage and avoids dominant 1/f noise from the active devices. Both works use differential topologies to reject common mode noise. In [15], an analysis of noise contribution for analog front end has shown that the primary noise contributors comes from the photodiode current, transimpedance amplifier noise, and switching noise in the switch capacitor circuit. Based on this, to improve SNR at the output, the noise contribution from the transimpedance amplifier and sample and hold should be minimized. Based on these characteristics and the circuit architectures presented in [13] and [14], we present our proposed system architecture composed of a transimpedance amplifier (TIA), sample-and-hold circuit, 2:1 multiplexer to toggle between glucose and oxygen sensing inputs, a single-ended to fully-differential converter, an ADC, and a wireless transmitter. The portion boxed in yellow designates what will be designed for the course.

II. SoC SYSTEM ARCHITECTURE

A. Transimpedance Amplifier

Since the photodiodes will provide a small current, adequate amplification is required to bring it to a usable range for signal processing. As the first amplifier in the overall system, the noise from this stage determines the overall sensitivity of the
entire chip. Transimpedance amplifiers (TIA) have been shown to provide high gain and low noise that is suitable for biomedical applications (see [16]-[19]). In a TIA, transimpedance gain on the order of MΩ has been reported in [16]-[19]. However, there exists a tradeoff between the gain and bandwidth of the amplifier. In addition, low noise techniques such as correlated double sampling (CDS) ([18]) and chopping ([14]) are commonly used. To reduce the bandwidth requirement, integrator-based TIAs have been designed for high gain in [16]. Table I defines state of the art performance and our specifications for the TIA.

### TABLE I: Comparison of State of the Art TIA

<table>
<thead>
<tr>
<th>[17]</th>
<th>[18]</th>
<th>[19]</th>
<th>Our Specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>112/83</td>
<td>158</td>
<td>184</td>
</tr>
<tr>
<td>Input Referred Noise(A_{ref},rms)</td>
<td>0.427pA\sqrt{Hz}</td>
<td>0.4pA\sqrt{Hz}</td>
<td>0.4pA\sqrt{Hz}</td>
</tr>
<tr>
<td>Bandwidth (Hz)</td>
<td>2MHz</td>
<td>40kHz</td>
<td>20kHz</td>
</tr>
</tbody>
</table>
| Circuit Techniques | Shunt- | CDS Switch | High gain 3- | CDS Switch-
| | /Current- | capacitor | stage TIA | capacitor |
| | Mode | TIA | TIA | TIA |

B. Single-Ended to Fully Differential Converter and Multiplexer

Since both glucose and oxygen need to be monitored, a multiplexer is required to switch between inputs. To accomplish this we will use a 2-to-1 mux using transmission gates. It can be controlled with a generated clock. The area and power consumption of this mux will be minimal for the overall design.

The single-ended to fully differential converter will take the output of the sample and hold from the TIA and provide a differential input to the ADC. This will be accomplished using a switched capacitor circuit as seen in [20]. Since our system architecture already supports switched capacitor circuits it can be accommodated.

C. Clock Generation

For our signal chain a clock generation block is required to control the switched capacitor circuits. Therefore we must develop dual nonoverlapping clocks. For the clock generation we intend to use a relaxation oscillator due to the simple design and low power operation. The relaxation oscillator can be implemented on-chip to generate clock frequencies on the order of MHz. In addition, we can use flip-flop based frequency dividers to create smaller frequencies if necessary. To facilitate this project we intend to design a 1 MHz relaxation oscillator.

D. 1st Order Switch Capacitor Sigma-Delta ADC

Once the signal has been captured and amplified by the analog front-end, the voltage representation of the fluorescence signal will be digitized and sent to the communication block of our SoC. The most commonly utilized ADC types in industry and academia are the flash, dual slope, successive approximation (SAR), pipeline, and ΣΔ ADCs. Considering trade-offs between complexity, power consumption, speed, resolution, and size, we will implement a 1st order switch capacitor ΣΔ ADC. This type of ADC achieves a very high resolution and low power at the expense of speed. Our system will operate in an open-loop configuration and, therefore, speed is not a stringent requirement in our design. Moreover, minimizing power consumption and increasing bit resolution is of extreme importance since the fluorescence signal is on the order of nanoamperes. In addition, ΣΔ ADCs perform the function of noise shaping by moving the low frequency noise to high frequencies outside the bandwidth of interest, thus allowing for the acquisition of very low frequency signals with a high degree of accuracy. We estimate that a 9-bit resolution for our ADC will give us enough accuracy from 20pA to 10nA to detect changes in the fluorescence of 1 part in 500.

### E. Wireless Transmission Link

To build the full SoC beyond the scope of ECE6414 a wireless transmitter is required. For data transfer, we envision a wireless transmission link operating in the ISM band at 915MHz. The transmitter block will consist of a Tristate Class-D amplifier driving a surface mounted antenna (Johnson Technology). The Class-D amplifier will be driven by a voltage controlled oscillator (VCO) implemented with a closed loop phase-locked loop (PLL) for frequency stability, as a result, our system will not need off-chip components for the wireless link. The closed-loop PLL implementation will also result in a more robust wireless link.

### F. Power Budget & Group Logistics

#### TABLE III: Division of Work

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Power Budget</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIA</td>
<td>15mW</td>
</tr>
<tr>
<td>Mux to Differential</td>
<td>1mW</td>
</tr>
<tr>
<td>Clock Generation</td>
<td>5mW</td>
</tr>
<tr>
<td>Multiplexer</td>
<td>1mW</td>
</tr>
<tr>
<td>ADC</td>
<td>10mW</td>
</tr>
<tr>
<td>Wireless Link</td>
<td>30mW</td>
</tr>
<tr>
<td>Total Power</td>
<td>62mW</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Member</th>
<th>Responsibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>Moez</td>
<td>TIA, Mux, S/E to Differential</td>
</tr>
<tr>
<td>Edgar</td>
<td>ΣΔADC</td>
</tr>
<tr>
<td>Sunil</td>
<td>Bias Generator &amp; Clock Generation</td>
</tr>
</tbody>
</table>
REFERENCES


