Georgia Institute of Technology
SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING
ECE-6414: Analog Integrated System Design – Spring 2015
1:05pm – 1:55 pm, Mon, Wed, Fri, CoC 16
http://www.ece.gatech.edu/academic/courses/ece6414/S15

Instructor: Maysam Ghovanloo, Ph.D. (mgh@gatech.edu), Phone: (404) 385-7048

Office Hours: Thursdays 1:00-3:00 pm, other times with prior appointment

TA: TBD


Other References: (recommended)
   P. Gray & Meyer
2. Design of Analog CMOS Integrated Circuits
   B. Razavi
3. The Art of Analog Layout, 2nd ed.
   A. Hastings
4. Analog Integrated Circuit Design
   D.A. Johns and K. Martin

Prerequisites: Analog Electronics (ECE-4430 and 3400 or equivalent), Co-requisites: None

It is assumed that you are familiar with the following topics:
1. Circuit theory, frequency response, small signal modeling and analysis
2. Solid-state devices and microelectronic circuits: P-type and N-type semiconductors, PN junctions, bipolar junction transistors, and MOS field-effect transistors (MOSFET).
3. Analog circuit building blocks such as current mirrors, reference generators, single and multi-stage amplifiers, differential amplifiers, and OpAmps.
4. Knowledge of MATLAB and CAD tools, such as SPICE or Cadence.

Course Description:
This semester, the course project and all its components, which constitutes 50% of the final grade will stay the same as previous years however, the structure of the lectures will be a combination of online video lectures, reading assignments, collaborative homework, and in-class activities, discussions, and a variety of active learning interactions among the instructor and students within and between their teams. I will employ an evidence-based active learning approach to teaching based on sound research in the field of education because it is shown to
result in a better learning experience for you. We will move further away from a passive learning environment, where a large number of students in class are not fully engaged all the time. There will be little emphasis on memorization of equations, derivations, and problem solving tricks that work for textbook problems and tests but break down when you apply what you have learned to different kinds of real life problems.

Since you will actually receive and watch the lectures online, ahead of the class, we will spend the class time on peer learning, which is shown by numerous research studies to be effective because it turns out that the best teacher of a new concept is someone who is also just learning it. Furthermore, having to explain a concept to someone else is the best way to reinforce your own knowledge of that concept. My role is to be your guide and coach, and to structure the learning environment to make sure this happens. Since this is the first implementation of this approach in ECE6414, it may not be perfect. However, with continuous and timely feedback from you, and close monitoring of the class performance/progress, proper adjustments will be made to make it a success, while having a fun and rich learning experience throughout the semester.

After a brief review of the prerequisites, we will look at some of the more advanced analog building blocks such as fully-differential OpAmps and dynamic analog circuits. We will use analog IC building blocks to construct simple analog IC systems such as data converters, filters, mixers, etc. We also review the characteristics and specifications of such analog and mixed-mode circuits from the system design perspective. This course is highly design/project oriented and emphasizes on intuitive understanding of circuits, particularly those topics used in analog ASIC design. As such, it requires sufficient time to be spent on watching the online videos, reading the assigned text, understanding the course materials, and applying them to the course homework and projects. In return, this course will provide you with valuable hands-on experience as you go through a real analog ASIC design cycle from the basic idea and circuit/system specifications derived from a real application to a complete functional schematic, layout of at least a major block on the ASIC (often the data converter) and detailed post-layout simulations. Organization, attention to the details, engineering compromise, optimization, time management, collaboration, effective communication, good presentation skills, and teamwork, which have proven to be important in analog integrated system design, will be practiced.

Aside from the time commitment and activities related to the course project, you will need to do a lot more preparation prior to class, but the time you will spend doing homework is reduced because you will complete them in groups. This style of teaching is actually a greater workload for me as well, because it is more difficult and time consuming to plan the in-class collaborative learning activities than it is to simply give lectures. However, towards the goal of creating the best learning environment, I am willing to take on this challenge. You should also carefully consider your other time commitments and workload before deciding to take this course.

**Topical Outline:**

Introduction, Review of analog IC building blocks
Noise analysis in analog circuits
Advanced current mirrors, amplifiers, and filters
Switched-capacitor circuits
Fully differential and high performance OpAmps
High speed comparators
Digital-to-analog converters (DAC)
Analog-to-digital converters (ADC)
Nonlinear analog circuits and mixers

Project Timeline:

Course Project and Teams:

Groups of three students should form a team and choose an analog system of their choice using a variety of key analog and mixed-mode circuit blocks that are discussed in this course, based on specifications derived from a particular application, preferably in bioengineering or life sciences. Based on my experience, forming a cohesive, balanced, and functional team is one of the most important factors affecting your grade. The same way that in real life you don’t necessarily have a chance to pick your colleagues, it is important for you to learn and adopt the necessary skills to effectively work with your other peers in class, who all share the same objectives at least over the course of this semester, which are learning the course materials and earning a good grade. This usually comes down to being responsible, understanding, and committing your fair share of time and effort towards the course project and other team assignments. Please also note that part of the grade associated with each team activity will come from your teammates.

Occasionally it would be acceptable for two or even three teams to each work on a sub-system of the larger analog system, provided that there would be sufficient variety of analog building blocks in each sub-system. Teams are encouraged to consult with the instructor in choosing their topics. Each team proposes their project topic in a 2-page draft by Draft-1 deadline (about 4 weeks through the semester). Draft-1 should include a rough block diagram of the complete analog/mixed-mode system showing the inputs and outputs of each block, on-chip and off-chip components, as well as the inputs/outputs of the entire system. It should also include a brief description of the biomedical application and any relevant online or published references that the group might have visited along with sufficient design specifications for each block to justify its suitability for ECE6414. It should also indicate the tentative role and responsibilities of each team member. Each team should select one of the members as the main point of contact with the instructor. A separate page can be dedicated to the list of references that the team has found and studied to come up with the project idea (advice: do not include a reference unless you have read it). It is also a good idea to find and understand the state-of-the-art in that area. Even though your specs in this class project do not need to push the limits.

After receiving approval from the instructor, team members perform a thorough literature search on their selected topic, and come up with more specific analog ASIC design ideas for the building blocks, detailed specifications, and the functions that they would serve in the system and eventually for the selected application. A summary of the literature survey, a detailed system block diagram, selected circuit topologies, and design targets for each block should be included in a 2nd Draft, and turned in by Draft-2 deadline (about 6 weeks through the semester). The page limit for Draft-2 is 7 pages including all figures but not references. System level simulations
using ideal circuit components in Cadence, MATLAB, Simulink, or any other CAD tool is highly encouraged at this stage to demonstrate the functionality of the main idea, identify potential challenges, and also guide the team towards a more accurate estimation of the required specs for each building block.

Please note that ECE-6414 does not include any CAD tool training. In case you do not have sufficient prior background in using CAD tools, particularly Cadence, please make sure to go through online tutorials and consult with the other team members. Draft-2 should include a table summarizing the “Design Specifications”, including the desired design targets, and preferably the state-of-the-art. It can also include a column showing the simulation results up to that point. The instructor will provide each team with individual feedback on Draft-2.

At this stage, team members continue implementing their ASIC designs at the transistor level, including layout and post-layout simulations, using Cadence tools. All ASIC designs should use the ON Semiconductor 0.5-μm standard CMOS process (C5N). Detailed information about this process and transistor models are available through MOSIS website (www.mosis.com/on_semi/c5/). This process operates reliably in 3-5V supply range. Using low voltage circuit design techniques, operation at lower voltages is also possible.

Considering the significance of the ASIC layout in the performance of analog circuits, important layout design techniques that affect the circuit performance in terms of matching, minimizing parasitic effects, and linearity, will be covered in class. A major portion of the proposed circuit/system, at least the data converter block, should be carefully laid out, following these layout design guidelines. Part of the project grade is dedicated to the quality of layout and post-layout simulation results. If your team plans to tapeout the ASIC for fabrication by MOSIS, your entire layout, including pad frame and protection circuitry should fit within half of a MOSIS “Tiny Chip” standard size, which means 1500 x 750 μm². Every two teams will be sharing one 1.5 x 1.5 mm² Tiny Chip.

There will be a Design Review about 6 weeks after Draft-2, at the time when all circuit schematics at transistor level should be complete and fully simulated. The instructor will review the simulation results for each design along with the team members at a computer station and provide them with feedback. Part of the simulation results will be graded at this stage.

The team members will have a chance to modify and improve their circuit designs during the last month of the semester as they layout their designs and observe the performance of their circuit blocks more realistically in post-layout simulations.

All the schematic modifications, simulations, and layouts have to be completed by the last day of classes, which is indicated as the “Post-layout Simulation” date on the course schedule. The instructor may hold a second design review on that day and review the layouts and post-layout simulations with the team members. The top-level schematic and layout of the ASIC design should pass design rule check (DRC) and layout vs. schematic (LVS) test.

Finally by the end of the semester each team will turn in a report that should follow the IEEE standard journal format (http://www.ieee.org/documents/trans_jour.docx). This paper should include a summary of the literature survey, complete design, design theory and calculations, complete circuit schematics, circuit layout, pin-out diagram, post-layout simulation waveforms, testing and measurement procedure (assuming the chip has been fabricated), and a table summary of the circuit characterization results (through post-layout simulations). Links to the
IEEE general information for authors is provided on the course webpage. There, you can also find template files for MS-Word. The page limit for your final paper is 10 pages, excluding the list of references. This is the only portion of the paper that will be graded based on completeness and quality of your writing. However, each team can add an unlimited number of appendixes to fully document their work.

During the final exam date/time, each group should present the entire project in a 15-min slide presentation (~15 slides) for the rest of the class in a conference style session. This session will be open to the public audience. Other faculty members and/or senior graduate students might be invited to evaluate the projects. The entire group should participate in the presentation and will be asked questions for 5-min by the instructor and other audience after their presentation.

To assess the individual participation of the team members, each member of the team will be asked to fill out an individual effort and collaboration assessment form about the other team members. This feedback is taken very seriously and also affects the class participation grade.

Those teams with the best functional circuit designs, based on post-layout simulations and other performance measures, will be given a chance to further complete their ASIC designs and submit their layouts through MOSIS Educational Program (MEP) for fabrication. The actual tapeout date, according to the MOSIS schedule for the ON-Semi 0.5-μm process, is going to be 7/13/15 (https://www.mosis.com/db/publ/fsched?org=ON-SEMI&year=2015).

The fabricated chips are expected to be back by mid October 2015. Team members are encouraged to fully test and characterize their ASICs after fabrication. Functional devices will be considered for additional experiments in their particular biomedical applications. If successful, measurement and experiment results can potentially be considered for submission to a professional conference.

Here are further important details about the projects:

- You may discuss questions in large groups, but during the final presentation, each person must independently answer questions related to the entire project. Therefore, each member of the team should be well aware of all the details of the ASIC design and its application. Also the grading will not be the same among all members of each team.

- For the final presentation, you should describe the background for your system (literature search results), state-of-the-art, methods, simulation results, challenges, and solutions. Please note that quality of your slides and presentation skills do matter. One should use fonts that can be visible when projected. One should minimize the number of slides with text only (I would strongly prefer no slides with text only, other than a conclusion slide at the end). Do not use schematics on black background. Do not use curves with thin lines or numbers on the axes with very small font that are hard to read. Results should be word-processed (avoid hand drawn / hand written materials).

- All project related materials are due electronically by email to the instructor (mgh@gatech.edu) at the beginning of the class on the day that they are due. In the e-mail please identify name (of all people in the team), as well as on the first slide, so that I know who should get credit for the project. Projects handed in after this deadline and before the beginning of the next class lecture will be graded from 50% of the full grade. After the beginning of the next class, no project will be accepted. This policy is firm, so do not fall behind! The workload will not get any lighter later in the semester.
• Only one set of slides will be accepted per team. To help me archive the presentation files, please use this naming convention:
  Team#_Draft1_ECE6414_S15.ppt
  Team#_Presentation_ECE6414_S15.ppt
• Try to add a relevant title for each slide and add a brief description so that your slides would be self-explanatory. Also try to add one or two slides at the end as a conclusion.

Class Attendance:
Attendance in class is required, even though I will not keep track of class attendance. However, you are highly encouraged to attend all class and makeup sessions. Because there are weekly quizzes that will be discussed in class, there are many other discussions and interactions in class that are not covered in the notes or textbooks.

Online Video and Reading Study Assignments and Weekly Quizzes:
Reading/study assignments include watching online instructional videos (2 or 3 per week) http://cmosedu.com/videos/cmos1/cms1_videos.htm, associated sections of the textbook, some journal papers, supplementary notes, literature search, and online articles that are related to each lecture and the course project. All assignments for each week will be posted on the Assignments page on the course website. Each week there will be a quiz (often on Mondays) from the online instructional videos and reading assignments to ensure everyone keeps up with the pace of the class and review the course material ahead of time. You will take the quiz individually on your notebook or tablet for 15 min and submit your answers. Then you will discuss it among your team for 15 min, and then submit again. Class notes and supplementary notes, which topics may or may not be included in the textbook, will be posted on the class webpage (calendar) and it is your responsibility to print them out and bring to the class with you. These materials will not be handed out during lectures. Students are responsible for both online and in-class lectures materials and reading assignments for the midterms and final project.

Each quiz also contains a feedback question, asking what was the hardest concept in the week’s study material. This will allow me to focus on the topics you most need help with. Therefore, as you complete the videos and readings, you can think about what are the topics you would like more clarification on, and I will try to emphasize them in class during the rest of the week. In accordance with dead week policy, there will be no quiz on the last Monday of classes.

Homework:
Homework will be assigned to each team, as seen on the course webpage. The homework will include designs, hand calculations, and computer simulation problems. The team members are free to divide the homework problems among themselves or each solve all of them individually and then compare their solutions. At the end, the team returns only one set of homework on the due date, electronically in the form of a PDF file: Team#_HW#_ECE6414_S15.pdf

Homework in this course is peer-reviewed/graded. The instructor collects all the homework and assign the PDF files from each team to another team on a random basis for each problem set. Members of each team will grade the other team’s homework and collectively write a max 1-page summary of what the other team should note or what they have learned from their mistakes. The instructor will assign the final homework grade based on a combination of the grade that
each team has received and the summary that the team has provided after grading the homework of another team. You are highly encouraged to first complete the problems individually because variations of those problems could be used in the exams. You are also encouraged to thoroughly grade your peers’ homework and provide helpful summaries because will learn a great deal from their mistakes. Each team member will also evaluate his/her teammates in terms of participating in completing and grading homework at the end of the semester.

Exams:

- There will be two closed-book, closed-note midterm examinations, each of 50 minutes duration. You can only have one sheet of notes (both sides), last exam’s sheet of notes, and a calculator.
- Each exam is cumulative: Every unit builds on all the previous units.
- Expect the unexpected: The exam will be over material covered in lectures (primarily), handouts, and in the textbook, but I reserve the right to make any/all problems not look like homework problems. I expect that you get the intuition of the key concepts from the homework. In the exam, you should be able to apply these concepts to different problems.
- All grades become final one week after they are returned in class.

Missed Exam and Quizzes:

If you miss a midterm exam or more than one quiz, or do not attend your project presentation without a certified medical excuse or my prior approval, a zero will be averaged into your grade. Certified excuses and prior approval will be dealt with individually. Generally, only one makeup exam will be held at a designated time near the end of the semester and before the final exam. This means that there will be only one make-up test, independently from which exam/presentation you miss. Thus, the make-up test will be comprehensive. To request an excused absence, 1- write a formal letter to me (typeset), dated and signed, stating your specific request and the reason you are asking for an excused absence; 2- provide documentation supporting your request; 3- bring this letter and the documentation to me in person before the requested date (if an absence is foreseeable) or within one week after the absence (if it is of unforeseeable nature), at which time your request will be discussed. Special cases will be dealt individually.

Academic Integrity:

It is the responsibility of the instructor to encourage an environment where you can learn and your accomplishments will be rewarded fairly. Any behavior which compromises the basic rules of academic honesty as described in the General Catalog will not be tolerated. It is the instructor’s understanding that the student’s signature on any test or assignment means that the student neither gave nor received unauthorized aid. For more information:
http://www.honor.gatech.edu/content/2/the-honor-code

Disabilities:

Reasonable accommodations will be made for students with verifiable disabilities. To qualify for these accommodations, students must register with Access Disabled Assistance Program for Tech Students (ADAPTS). For more information: http://www.adapts.gatech.edu/
**Grading Policy:**

This class is not graded on a curve, but on an absolute scale. However, the grade scale may be adjusted if there is a significant need. The grading is often based on active and honest participation in class and quality of the final project, presentation, and the paper, and not just correct answers in the exams. I would like you to focus on learning, not on the grade. Since you will be collaborating with others quite often, it is in everybody’s best interests to work together.

<table>
<thead>
<tr>
<th>Component</th>
<th>Weight (%)</th>
<th>Grades</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework</td>
<td>15% (4-6)</td>
<td>A: 90 – 100  B: 70 – 89</td>
</tr>
<tr>
<td>Midterm-1</td>
<td>10%</td>
<td>C: 50 – 69   D: 40 – 49</td>
</tr>
<tr>
<td>Midterm-2</td>
<td>10%</td>
<td>F: 0 – 39</td>
</tr>
<tr>
<td>Quizzes</td>
<td>15% (12-15)</td>
<td></td>
</tr>
<tr>
<td>Project</td>
<td>50%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>+ Up to 5% extra credits for active participation in class and useful feedback</td>
<td></td>
</tr>
</tbody>
</table>

**Project Grading:**

- Draft-1: 5% Circuit performance 10%
- Draft-2: 10% Presentation 20%
- Layout quality/techniques: 10% Final Paper 30%
- Simulation results: 10% Group cooperation 5%

**Extra Credits:**

Extra credits will be assigned to groups with innovative ideas in their ASIC designs, resulting in higher than expected performance. Also groups that complete the layout, post-layout, and corner simulations for their entire ASIC will receive extra credit.

Active participation in class and providing useful feedback that would lead to improved class performance will be rewarded with extra credits. An important aspect of learning is reflection, or knowing the balances of your strengths and weaknesses, and understanding how the learning you have achieved has changed that balance. Along with Draft-1, turn in, via email to me, a 1-page (single spaced, single sides, 11-pt font, 1 inch margins) your “Personal Course Goals”. This is an open-ended statement, but you may choose to address any combination of the following questions: 1- What do you want to learn from this class? 2- What strengths and weaknesses will you bring to the team interactions? 3- What academic weaknesses would you like to address in this class? 4- How do you think you might apply the knowledge learned from this class in the future? 5- What applications of ASIC design are you most interested in?

Then, anytime starting dead week until the final exam, you may turn in a marked-up version of the same “Personal Course Goals” document by email. You should comment on how your original goals and expectations at the beginning of the semester compared to your actual experience, in a separate page. This opportunity will only be available to those that completed the original self-evaluation along with Draft-1.

**Auditing Criteria:**

The ECE department does not grant any auditing credit. However, if you are interested in just sitting in the class, please contact me.

**Course Webpage and T-Square:**
All the important course announcements and notifications will be posted on the course webpage, [http://www.ece.gatech.edu/academic/courses/ece6414/S15](http://www.ece.gatech.edu/academic/courses/ece6414/S15), and you are encouraged to check it daily. Please also register for the T-square site for this course, ECE6414-A. All the grades will be posted on T-Square. You will also take all the quizzes online on T-Square.

### Course Schedule (Tentative):

<table>
<thead>
<tr>
<th>Exam/Project</th>
<th>Date</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Project Draft-1</td>
<td>Monday 2/2/15</td>
<td>In class</td>
</tr>
<tr>
<td>Midterm-1</td>
<td>Monday 2/23/15</td>
<td>In class</td>
</tr>
<tr>
<td>Project Draft-2</td>
<td>Monday 3/2/15</td>
<td>In class</td>
</tr>
<tr>
<td>Design Review</td>
<td>Friday 4/3/15</td>
<td>4-6 pm</td>
</tr>
<tr>
<td>Midterm-2</td>
<td>Wednesday 4/15/15</td>
<td>In class</td>
</tr>
<tr>
<td>Final Papers</td>
<td>Saturday 4/25/15</td>
<td>12 am</td>
</tr>
<tr>
<td>Final Presentations</td>
<td>Monday 4/27/15</td>
<td>2:30 - 5:30pm</td>
</tr>
</tbody>
</table>