Summary By Saad Bin Nasir

HW#3 helps us learn the following key components

Problem one helps us understand the distribution of vds on the output transistors of an amplifier. Improved biasing can be made in this problem by distributing supply voltage equally on all of the transistors on the output branch. One such biasing can be based on a current source as presented in solution of problem one.

Problem two helps us in understanding the trade-offs involved in putting gain boosting in an amplifier. This can bring along a potential problem of instability as we are increasing the number of feedback loops involved in the overall amplifier. Adjustment of CMFB gain is another important part of this problem.

Problem three helps in changing the biasing of the circuit to operate at a lower VDD but it comes at a cost of increased power.

Problem four is the implementation of an SC integrator. This problem helps us identifying the trade-offs involved in implementing an amplifier whose input and output common mode levels are not same. Therefore, we cannot short them during the hold mode.

Problem five addresses the issue of increasing the output swing of an amplifier at the cost of increased power consumption and reduced gain. Biasing can become really challenging in such scenarios as we can encounter nonlinearity in the gain.

Problem six is the simulation of a comparator which can operate rail to rail by introducing PMOS and NMOS diff pair based folding. Here we analyzed the comparator offset and the kickback noise.

Suggestions to Faisal on his HW

Please see how the circuit is sensitive to biasing errors as the gain becomes nonlinear. Derivative of time domain signal should give the peak gain right at the crossing of the two output signals of the diff pair.
Report for Assignment 3
Submitted by: Mohammad Faisal Amir

I checked Gregory Erwin’s assignment. He scored 98/100.

The first problem required students to critically analyze a provided circuit and suggest modifications to it to improve the performance. The second problem examined the students’ understanding of gain enhancement, a concept previously introduced, and required them to apply the concept to a differential op amp as well as the common mode feedback. Students were also required to judge the performance of the circuit through various simulations.

The third problem suggested a modification to an existing topology and asked students to analyze the advantages and disadvantages through the required simulations such as step response, gain and power consumption.

The fourth problem brought forward a switched capacitor CMFB and required students to show the operation of a switched capacitor integrator.

The fifth problem replaced the bias circuit and examined its effects on the op amp through the pertinent simulations.

Finally the sixth problem required analyzing a comparator and judging its performance in terms of various parameters such as the sensitivity, common mode range and kickback noise.

Aside from a minor omission in the first problem, Gregory was quite adept at providing the required answers through simulations, as well suggesting ways to improve the performance of the required circuits, which resulted in him obtaining a high score.
Comments for my classmate – Peter McMenamin

- Problem 1
  o OK
- Problem 2
  o OK
- Problem 3
  o OK
- Problem 4
  o OK
- Problem 5
- OK
- Problem 6
  o Is missing
  o To calculate kickback noise, you can refer to figure 16.37 and the associated discussion.
  o For sensitivity, easiest way is to have an input voltage constant and have the second input voltage as a pulse. You can analyze the sensitivity by looking adjusting the Peak-to-Peak value of the second input and see how the output changes.

What I learned:

- Better understanding of differential amplifiers with CMFB
- Gain Enhancement pros and cons
- How to make the op-amp stable for lower VDD, and the disadvantages
- Create Switch Capacitor Integrator and how to characterize them
- Comparator characterization (how to simulate for kickback noise and how to determine the sensitivity)
HW3 Summary

**General Summary of assignment (what was learned)**

- This homework provided a good overview of fully differential operational amplifiers.
- Working almost entirely with the short-channel process was a good experience. Small changes in channel length or biasing can have huge effects on circuit response.
- It seems much more difficult to achieve good slew rate and stable step response with these technologies and topologies than with single-ended long-channel op amps.
- Different problems utilized different CMFB configurations in different ways, and seeing the effects of these different configurations was quite useful.
- The SC integrator problem provided a good practical example of how a fully differential op amp might be used in a circuit.
- I would have preferred a few more problems that involved modifying individual transistor problems to achieve a desired response rather than all problems comparing different topologies and giving the exact schematic to be used.
- Several of the problems were comprehensive in that they referenced/required material from Ch. 25 to be correctly implemented.

**Notes on Graded Homework (Zehua’s)**

- I have excluded pages containing the netlists from the final graded submission since I didn’t want to scan that many pages.
- Only glaring issue is the lack of compensation for gain enhancement amplifiers in problem 2. This may be responsible for the step-response issues appearing in the simulation.
- For the comparator problem, it might have been good to test a larger range of inputs to see just how far above/below the rails the ICMR extended.
- Brief summaries of important parameters (e.g. loading used for testing step response) would have been nice rather than having to read through netlists.
- Everything else appears correct.
1. Baker 26.7
   That is correct as best I can tell. It's interesting that the NMOS “tunes” the voltage distribution.
   **Points awarded: 10/10**

2. Baker 26.15
   I had similar results. It's interesting to see that the fully-differential op-amp has very low gain
   **Points awarded: 20/20**

3. Baker 26.16
   What was the W/L that you decided on? It looked like a W/L ratio of 10/3 worked best for me.
   **Points awarded: 15/20**

   Nice simulation results!
   **Points awarded: 20/20**

5. I got similar results. It seemed the new bias circuit very much degraded the overall performance.
   **Points awarded: 20/20**

6. Baker 27.4
   Very nice comparator for a wide-range of applications!
   **Points awarded: 10/10**
ECE6414 HW3 Summary

Zehua Guo 902742161

For myself:

Output common-mode voltage of the first stage can be used to bias the second stage.

Adding a current source branch can help regulating $V_{DS}$.

Gain-enhancement op amps need to be compensated as well.

For David Fleischhauer:

Digital logics should be kept at minimum size.

Output common-mode voltage needs to be kept at half of the supply through CMFB.
Summary

Problem 26.7 [10/10]
In this problem, the key point is to evenly distributing Vds, which makes the circuit can work in a lower Vdd.

Problem 26.15 [15/20]
In this problem, a gain enhancement topology is used to increase the DC gain. However the tricky point is, for the four diff-amps, a buffer is need in the first stage to shift the common-mode voltage to the ICMR range.

Siwei made a mistake in the connection of the bulk of the PMOS and NMOS.

Problem 26.16 [18/20]
This problem is a practical realization of the first problem. By evenly distributing Vds, this circuit can work at a lower Vdd, but it consume more power.

Problem 26.19 [17/20]
This Problem helps me to further understand the CMFB between the two stages. When design the circuit, I carefully tuned the parameters in order to the output waveform has a enough gain. The vpp of the output in Siwei’s homework seems to be too low.

Problem 5 [20/20]
Siwei has done a good job.

Problem 6 [10/10]
Siwei has done a good job.
Things I learned from this assignment:

When adding noise sources in parallel, it is better to use noise currents than noise voltages, so convert the noise to the 4KT/R current whenever there’s a node with several resistors attached.

That said, one thing I learned from grading Adam’s homework is that there are multiple ways to accomplish the same goal. In particular, adding noise voltages in parallel can be accomplished with superposition, and has the advantage of being a much more intuitive method than the one described in the book, in part due to the following note:

It’s important to pay attention to node voltages when determining the path of noise current. For example, whenever an op amp holds a node at zero volts due to the virtual short between its terminals, it’s likely that the noise current due to the input resistor will only travel through the feedback network because the far end of the input resistor is tied to the source voltage, which gets shorted whenever you analyze noise. If the voltage at both ends of a resistor are the same, no current (even noise) will flow through it.

In LT spice, I learned how to perform noise simulations, something I had never done before, and I became more comfortable with using voltage controlled voltage supplies. Lastly, I discovered that CTRL + left clicking the name of a plotted trace allows you to integrate that function over some bandwidth, which is important for determining RMS noise from PSD.

Comments for Adam:
As indicated on the graded homework, you can approximate the RMS value by integrating over a definite integral of sufficiently large bandwidth, and in that way avoid crashing LT spice.
Summary for Lian Duan’s Homework 3
By Siwei Wang
Overall score: 92/100.

1. Baker 26.7
   [10/10] Correct
2. Baker 26.15
   [20/20] Please put the circuit diagram in the homework.
3. Baker 26.16
   [17/20] Wrong circuit figure on the first page? The circuit on the second page is correct.

   Question: what’s the main advantage and disadvantage of CMFB in differential amplifier vs. in output buffer?


5. 
   [15/20] Please commend on the benefits and drawbacks of the new design.

6. Baker 27.4
   [10/10] Correct. Better if kickback noise can be simulated.
Comments on Saad Bin Nasir’s Homework #3
Tao Wang

Very great work and detailed simulation results attached.

The author has great understanding of analog circuit schematics and SPICE simulation. The quality of the homework is worth of 10 points.

All the voltage signals were simulated well, with output voltage response, differential output voltage response, and open-loop DC voltage gain.

The author understands well of the application of CMFB in fully-differential amplifier circuits, and know how to do the SPICE simulation and improve the circuit performance. The curves of SCFB for the amplifier and SCFB for the buffer were both plot in Problem #4.

In Problem #2, the author successfully achieved a high open-loop DC voltage gain of 2,700.

In Problem #6, the author simulated the Kickback noise and showed the rail operation.
Concerning problem 26.7, using a MOSFET as a current source and a diode connected MOSFET to make the VGS across all of the MOSFETs at around 200mV helps keep the circuit more uniform, operate at lower voltages, and is helpful when adding other op-amps to the circuit. This is done at the cost of a slight power increase and gain reduction. As for the fully differential opamp of problem 26.15, the added gain enhancement circuitry brings the gain up to over 2.4kV/V at the cost of added complexity and power consumption. I think it’s interesting that the gain of a fully differential op-amp by taking the derivative of the difference of the non-inverting and inverting outputs. There was no ringing in the transient step response. Biasing for lower voltage operation is the topic of 26.16. The added diode connected MOSFET has an aspect ratio of 10/50 to stabilize the op-amp. The switch-cap integrator 26.19 for some odd reason has a slow varying sinusoidal common-mode variation. Otherwise, the short term operation of the switch-cap integrator works well. The biasing circuit changes of problem 5 were pretty confusing. Assuming that the intention of the problem is to add Vbias1 and Vbias2 in addition to maintaining Vbiasn, a connection between Vbias2 and Vbiasn must be removed to avoid contention between the biasing circuits. Circuit performance is worse across the board. Alternatively, the circuit could be powered by only Vbias1 and Vbias2, in which case it pretty much doesn’t work at all. My advice here is to leave a good working design alone and don’t degrade the performance with added complexity. The ICMR of 27.4 indeed extends between the power supply rail voltages.
First problem displayed the technique to divide VDD among MOSFETS in differential amplifier. This is achieved by adding a current source through the central transistors.

Second problem showed how the total gain of opamp can be increased by using gain enhancement technique. However, this will add complexity to stability analysis and consume more power.

Third problem showed the effect of changing W/L of diode connected transistor on DC ad small signal performance of opamp. Fourth question displayed operation of switched capacitor based CMFB.

Fifth question shows implementation of wide swing differential amplifier with a new bias circuit. This design ensures the diff-amp output decreases when Vcmfb rises. The last problem shows the technique to increase the ICMR beyond power supply rails.

I graded homework of Kevin Mohammed. He forgot to show simulation results for Q2 and did not attempt Q4 and Q5. He solved remaining questions correctly.
Problem 1 – 6)

Overall your plots and schematics looked just like what I had, but I can’t read or determine what each plot is, or the values of your components. For this reason, I had to take off 1 point for each problem. Giving an overall score of 94.

What I learned)

What I learned from this homework is that switch capacitor simulations take a very long time to run. I would like to learn a better way to simulate these types of circuits, since I had the same issue with the project. I know you can run co-simulations with MATLAB and cadence together, but Georgia Tech doesn’t seem to have a license for this feature unfortunately.