Low Power, Low Noise Chopper Amplifier for EEG Acquisition

S. Devarakond, B. Narayan, H. Sane, J. Zaveri

Abstract—This paper describes a micropower chopper stabilized amplifier for sensing EEG signals. The 4-channel EEG system utilizes a chopper stabilized amplifier and digital acquisition system. The system consists of an analog multiplexer, modulator, chopper stabilized amplifier, demodulator, level shifter and SAR ADC implemented in 0.5\(\mu\)m CMOS technology. The above technique provides an innovative method for eliminating the low frequency noise of the system and efficient data acquisition of the Electroencephalogram (EEG) signals. The input referred noise of the chopper stabilized amplifier is 52.5 nV/\(\sqrt{\text{Hz}}\). The entire system consumes 850 \(\mu\)W of power with a supply voltage of +/-3.3V. The area occupied by the system is 0.75 mm\(^2\). The system output consists of 10 bits in sign magnitude format.

Index Terms—EEG, biopotential acquisition, flicker noise, chopper stabilization, SAR, ADC

I. INTRODUCTION

The demand for technologies that help neuroscientists and clinicians to actively observe a large number of neurons in the brain has increased significantly. Currently, the biopotential acquisition systems are bulky and not portable that makes it difficult for the on-going diagnostics and causes discomfort to the patient. There is a need to make these systems more compact and to extend their applications to various fields.

Commonly monitored biopotential signals are EEG, ECG, and EMG. Figure 1 shows the characteristics of these signals, and it can be seen that they have a very low signal amplitude and operate at extremely low frequencies (<150 Hz). This is a major reason their performance is limited by the offset and the noise of the input amplifiers. The physical origin of low frequency noise in MOSFETs can be defined from the carrier number fluctuation theory, or the trapping-detrapping model. It is caused by the fluctuation of the number of inversion layer carriers as they are trapped and detrapped to and from traps located in the oxide, and it accounts for the carrier number and the mobility fluctuations [1]. It should also be noted that the typical offset voltages for these applications is around 10 \(\mu\)V. Due to this low frequency and \(\mu\)V level amplitude of these signals, they are often dominated by noise. Also present are the common-mode interferences from the mains, as well as the electrode offset.

Some techniques that can be employed to remove the offset and the 1/f noise dynamically include chopper stabilization, autozeroing (AZ), and correlated double sampling (CDS). While the latter two mentioned are sampling techniques, chopper stabilization is a modulation technique that can eliminate the effects of op-amp imperfections. The chopper stabilization technique was first introduced in 1948 by E.A. Goldberg [2]. Earlier, the chopping techniques involved switched ac coupling of the input signal and demodulation of this signal back to the dc signal. While these amplifiers achieved very low offset, and very high gain, they had limited bandwidth and required filtering to remove the large ripple voltages generated by chopping. This problem was solved by introducing the chopper stabilized amplifiers that combined the chopper amplifier with a conventional wideband amplifier that remained in the signal path [3].

The chopper stabilization technique essentially uses an ac carrier to perform amplitude modulation on the input signal. A chopper stabilized amplifier system consists of modulating and demodulating carriers with period \(T = 1/f_{chop}\), where \(f_{chop}\) is the chopper frequency. It should be noted that the signal is bandlimited to half of the chopper frequency to prevent aliasing. Figure 2 displays the relationship between noise and frequency. As seen, the 1/f noise is dominant at low frequencies, and thus the low amplitude EEG signals are susceptible to noise from the CMOS transistors. Basically, amplitude modulation using

![Fig. 1. Frequency and Amplitude of Biopotential Signals [4].](image1)

![Fig. 2. Noise versus frequency [1].](image2)
odd harmonic frequencies of the modulating signal, leaving the chopper amplifier without any offset or low-frequency noise [4].

Therefore, designing the analog front-end is extremely crucial for these applications. In order to achieve the best signal extraction, a front-end with high CMRR, low-noise, and high-pass filter characteristics is required, with configurable gain and filter considerations. Hence this work describes a complete EEG acquisition ASIC with low power dissipation. This paper introduces a novel method by having a fully differential chopper stabilized micro power operational amplifier designed with a negative feedback that behaves like an inherent low pass filter, followed by a fully differential 10-bit successive approximation register ADC.

The structure of the paper is as follows. Section II describes the architecture of the EEG acquisition system. Section III describes the analog front-end followed by Section IV that describes the digital end. Section V then describes the various testing techniques and presents circuit simulation results after system integration. The last section then provides the conclusion and areas for improvement.

II. EEG Acquisition ASIC

The figure below shows the architecture of the ASIC. It consists of four readout front-end channels, a bias circuit, a 10-bit SAR ADC, an analog multiplexer. Each readout channel is selected by an external clock, and fed to the chopper stabilized amplifier. The chopper amplifier works at an $f_{\text{chop}}$ of 4 kHz. The capacitive loads are used as a negative feedback that actually behave like a low pass filter. The ASIC uses a 30 kHz external clock input from which the timing signals are generated by the on-chip digital control circuit. A 10-bit ADC is used to digitize the output from the amplifier. The bias circuit is built using the bandgap reference circuit topology. The ASIC has been implemented in 0.5µm CMOS process.

A. Analog Multiplexer

The advantage of an analog multiplexer is that it allows the use of a single amplifier to service multiple recording sites. The architecture used for the analog multiplexer is shown in figure 4. The input channels are Electrode 1- Electrode 4. The multiplexer consists of transmission gates that basically pass the signals when their respective clocks are triggered and are high impedance when the gates are turned off. Transmission gates were chosen to prevent charge injection and clock-feedthrough. The nmos transistors are $15/1.05$ µm, and the pmos transistors are $30/1.05$ µm.

B. Chopper Stabilized Amplifier

The basic requirements for the amplifier were low noise, low power, high CMRR, and a considerable gain.

A fully differential micro power amplifier was designed and implemented. The input signal from the multiplexer and a reference signal of known behavior act as inputs to the chopper modulator. The architecture used for the chopper modulator is shown in figure 5. Transmission gates were used again to avoid clock feed through issues. The chopping frequency used was 4 kHz. Typical values used in literature are in the range of 1 to 4 kHz. Higher frequencies can aid in eliminating $1/f$ noise as much as possible. One thing to note is that due to the switching action of the transistors, one will observe spikes in the signals. These spikes can be filtered using various techniques [3]. We used the filtering technique after demodulation to get rid of the high-frequency components.

III. Analog Front End

Since EEG signals operate at very low µV ranges, these signals are susceptible to large amounts of common-mode interferences, and thus a low-noise and high-CMRR amplifier is necessary for which chopping is commonly used. The analog front-end components include analog multiplexer, chopper modulator and demodulator, differential amplifier with CMFB circuit, level shifters and bandgap reference circuit.

A. Analog Multiplexer

The basic requirements for the amplifier were low noise, low power, high CMRR, and a considerable gain.

A fully differential micro power amplifier was designed and implemented. The input signal from the multiplexer and a reference signal of known behavior act as inputs to the chopper modulator. The architecture used for the chopper modulator is shown in figure 5. Transmission gates were used again to avoid clock feed through issues. The chopping frequency used was 4 kHz. Typical values used in literature are in the range of 1 to 4 kHz. Higher frequencies can aid in eliminating $1/f$ noise as much as possible. One thing to note is that due to the switching action of the transistors, one will observe spikes in the signals. These spikes can be filtered using various techniques [3]. We used the filtering technique after demodulation to get rid of the high-frequency components.

Once these signals are up-converted to a higher frequency, they are fed to the inputs of the fully differential micro power operational amplifier. The architecture implemented is shown in figure 6. The common-mode feedback circuit used is shown in figure 7.
Adaptive biasing can reduce power dissipation in an amplifier while at the same time increase the output current drive capability [5]. When the two inputs are equal, the currents in the side branches are zero and the diff-amp DC tail current is simply $I_{ss}$. If either the positive or the negative input increases, the currents on the respective side branches increase above zero, increasing the diff-amp tail current. Therefore, the maximum output current is limited to either $I_{ss} + I_{ss1}$ or $I_{ss} + I_{ss2}$. Power dissipation can be significantly reduced using this technique, and slew rate characteristics can be improved greatly. Therefore, the current is given by

$$I_{ss} + A((I_{ss1} - I_{ss2}))$$

where $A$ is the parameter that determines the gain of the amplifier.

These fully differential signals are then sent to the inputs of the demodulator which also has an $f_{chop}$ of 4 kHz.

A novel method of filtering is introduced in this paper. The chopper amplifier could give a large output resistance, and when combined with a large capacitive load, they could act as an inbuilt low pass filter, which eliminates the need to have a stand alone $GmC$ filter. The $GmC$ filters typically consume a large area and also dissipate large amounts of power. The technique follows that of the conventional RC filter around an active operational amplifier through a negative feedback. The capacitors can provide the necessary feedback to eliminate the high frequency components in the signals, and produce clean signals at the end of the demodulation. The values of the capacitor are listed in the table below.

### TABLE II
**Amplifier specifications after post-layout simulations**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Performance Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{F1}$, $C_{F2}$</td>
<td>14 pF</td>
</tr>
<tr>
<td>$C_{L1}$, $C_{L2}$</td>
<td>5 pF</td>
</tr>
<tr>
<td>Gain</td>
<td>70 dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>70 degrees</td>
</tr>
<tr>
<td>CMRR</td>
<td>-200 dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>-250 dB</td>
</tr>
<tr>
<td>Power</td>
<td>169.5 $\mu$W</td>
</tr>
<tr>
<td>Input referred noise</td>
<td>52.5 nV/$\sqrt{Hz}$</td>
</tr>
</tbody>
</table>

C. Level Shifter

The SAR ADC operates best when the differential signals have no DC offset. So a level shifter was implemented, the schematic of which is shown in the figure below. A simple technique was used to bring down the DC levels from 1.65 V to 0 V.

D. Bias Circuit

The bias circuit implemented is the Bandgap Reference Circuit [4]. This circuit is based on the thermal voltage self-biasing topology, and was chosen because it provides a high degree of supply voltage independence. The required voltage from the BGR is 1.65 V.

E. Characterization of the Amplifier

The amplifier was characterized using the four different process corners, and all produced similar results. The results of the characterization is provided in detail below.
The first figure gives the amplifier gain, followed by the phase. For the given range of frequencies, the amplifier is stable with over 65 degrees of phase margin. The next two plots provide the input referred noise after adding the choppers followed by the PSRR and common mode gain (or its ability to reject common mode) of the front end. It is important to note that the input referred noise before adding the choppers was almost an order of magnitude higher (800 nV/√Hz). The input referred noise reduced significantly after adding the chopper to about 57 nV/√Hz, and this value dropped further after post layout simulations to 52.5 nV/√Hz. This value is very comparable to those reported in literature, and even can be considered towards the lower end.

Figure 10 illustrates the chopper amplifier function. The input signal was 10 µV, and as seen from the image, it gets amplified, and the output signal is clean due to the filtering action.

IV. Digital and Processing End

The EEG system utilizes an ADC for performing digital back end processing. The ADC is designed using the fully differential Successive Approximation topology. Successive approximation (SAR) ADCs provide a feasible solution for low-power, high resolution, accurate applications. It only requires one comparator regardless of the resolution, and there is no latency for the internal clock of an SAR ADC, which works at all times once the conversion is initiated [11].

The major blocks involved in the architecture are the fully differential capacitive main arrays and a single resistive array, comparator, SAR digital logic, delay, trigger and reset blocks. The block diagram of the SAR ADC is as shown in figure 17. The SAR outputs a 10 bit (N) signed digital code. The capacitive arrays output the 6 significant bits (M) of the digital code and the resistive array provides the last 4 bits (N-M). A single R-DAC is utilized keeping in consideration the power consumption of the ADC circuitry.

The charge redistribution SAR ADC utilizes the capacitive array for Track/Hold as well as the DAC. The ADC digitizes the analog output in 12 clock cycles. The system is provided with an external as well as the internal clock working at 30 kHz and 400 kHz respectively. The sampled differential analog signal is provided to the comparator which outputs the signal to the digital logic. The above comparison of the analog signal is made with different DC voltages.

The principle of SAR ADC is based on the bootstrapping principle of the capacitor. The SAR ADC is initially reset using a global reset signal of the system. In the reset mode both the plates of the capacitor are connected to the ground. In the sample mode the top plate is connected to
ground and the bottom plates to the input voltages (bottom plate sampling is utilized) for all the capacitors except the capacitor corresponding to the MSB which is connected to $V_{ref}$. Hence the stored charge is given as:

$$Q_x = -C_{tot} \left(\frac{V_{in}}{2} + \frac{V_{ref}}{2}\right)$$

In the hold mode the top grounding switch is then opened and then the bottom plates are connected to ground. The redistribution mode commences when the MSB is grounded during its test, while all other capacitors are sequentially tested by connecting them to $V_{ref}$ initially and then based on the comparator output the switches are either connected to ground or $V_{ref}$ for one of the DAC arrays and the complementary signal is provided to the other DAC array. The equation governing the operation is given as:

$$V_x = -\frac{V_{in}}{2} + \frac{V_{ref}}{2} (-b_9/2 + b_8/2^2 + b_7/2^3 ..., )$$

If $V_x$ from the positive DAC array is greater than that of the negative DAC array the comparator switches to 1 and 0 for vice-versa. The detailed explanation of the operation is provided in [12].

Thus for a 1.65V reference obtained from the BGR, the input voltage range is in between -1.65 and 1.65 V. In our digital logic, MSB, which is the sign bit is 1 for a negative differential input voltage and is 0 for a positive differential voltage.

A. DAC

The capacitive DAC consists of a series of capacitors which are multiples of 2 (ranging from $C$ to $C/32$ in our case with the largest capacitor being 4 pf). The resistive binary weighted sub-DAC consists of a chain of resistors each of 50 k-ohm. The switches present in the main DAC as well as the sub-DAC are transmission gates used to minimize the clock feedthrough as well as input dependent charge injection. Since the ADC has an accuracy of 10-bit, the challenge involves in ensuring that the delay due to the resistances of the switches and the varied capacitances remain relatively constant. This was ensured using relative sizing of the transmission gates. The test case designed for the R-Sub DAC is shown below in figure 18.

The sampled input signal of 100 mV differential amplitude is digitized through charge distribution principle as shown in the next figure.

B. Comparator

The comparator consists of a pre-amplifier followed by a memoryless sense amplifier and an SR latch. The Comparator diagram is shown in figure 20.

The comparator works on clock and clock-bar signals which ensure memoryless operation by pulling the nodes of the comparator to known $V_{dd}$ and $gnd$ states. Thus the design implemented does not have memory effects and the final stage of the implemented circuit consists of a latch.
which holds the current state until the next state is obtained. The output of the comparator test bench is as shown in figure 21 for complementary input signals.

C. SAR Digital block implementation

The digital implementation of the circuit is shown in figure 22 and is a standard implementation consisting of D flip-flop followed by registers and SR latches. N-MOS and P-MOS switches are utilized to reset the signals.

An internal generated pulse triggers the circuit and based on the output generated from the comparator, each of the bit is switched.

The ADC test signal which consists of a single sinusoidal test signal of frequency 128 Hz is used and the output digital code corresponding to the digital signal is shown in figure 24, figure 25. There exists a change in the frequency of the signal due to the clock frequency not being an integer multiple of the input signal and due to variable transient nature of the cadence simulation environment.

The PSD of the ADC is calculated with 226 sampled and is shown in figure 27. Repeated averaging of the signal would provide better ENOB and SNDR results.

The characteristics of the ADC is listed below in the Table (III).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Performance Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Consumption</td>
<td>700 µW</td>
</tr>
<tr>
<td>SNDR</td>
<td>40 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>7</td>
</tr>
<tr>
<td>DNL</td>
<td>1.5 LSB</td>
</tr>
</tbody>
</table>

V. Integrated System

The schematic of the integrated system is shown in figure 27. The comparison of this work along with others is presented in figures 28 and 29. There were a trade-offs with respect to input referred noise and power and area, and an optimal value was selected that gave a good balance of the two. The fully differential SAR was designed based entirely on logic since there weren’t any designs discussed in literature. The final system results are discussed in Appendix 1.

Figure 30 gives a picture of the pad frame. The area of the chip is 0.81mm².

VI. Conclusion

A novel low power, low noise chopper stabilized amplifier for EEG acquisition was described. With area, power, stability, and portability as the criteria, different figures of merit for the analog and digital ends were obtained. The system was built on 0.5µm process, and it was implemented on a 0.81mm² chip. The system integration results were discussed. The novel techniques introduced in this paper were the use of micropower chopper stabilized amplifier that effectively reduced the input referred noise by an order of magnitude. The low pass filtering technique was also new, and it helped eliminate the unwanted high frequency noise. The high resolution fully differential 10-bit charge redistribution SAR ADC was also novel in its logic implementation, and provides significant resolution during the analog to digital conversion.

REFERENCES


Fig. 21. Comparator output check.

Fig. 22. Block Diagram of the SAR digital implementation.

Fig. 23. Test bench output for ADC

Fig. 24. Digital output codes of the first five bits in the ADC test bench setup.

Fig. 25. Digital output codes of the last five bits in the ADC test bench setup.

Fig. 26. PSD of the ADC.

Fig. 27. Schematic of the entire system with the Analog Front-End and Digital and Processing End.

VII. APPENDIX

A. Comparison Chart

Figure 31 gives the outputs of various stages after system integration.
Fig. 28. Input Referred Noise comparison chart.

Fig. 29. Power consumed by front-end.

Fig. 30. Padframe of the EEG Acquisition ASIC.

Fig. 31. System integration results.
ECE 6414 Team 4: Low Power, Low Noise EEG Acquisition System

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November 12, 2009
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Chapter 1

Introduction

The demand for technologies that help neuroscientists and clinicians to actively observe a large number of neurons in the brain has increased significantly. Currently, the biopotential acquisition systems are bulky and not portable that makes it difficult for the on-going diagnostics and causes discomfort to the patient. There is a need to make these systems more compact and to extend their applications to various fields.

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Some techniques that can be employed to remove the offset and the 1/f noise dynamically include chopper stabilization, autozeroing (AZ), and correlated double sampling (CDS). While the latter two mentioned are sampling techniques, chopper stabilization is a modulation technique that can eliminate the effects of op-amp imperfections. The chopper stabilization technique was first introduced in 1948 by E.A. Goldberg [3]. Earlier, the chopping techniques involved switched ac coupling of the input signal and demodulation of this signal back to the dc signal. While these amplifiers achieved very low offset, and very high gain, they had limited bandwidth and required filtering to remove the large ripple voltages generated by chopp-
This problem was solved by introducing the chopper stabilized amplifiers that combined the chopper amplifier with a conventional wideband amplifier that remained in the signal path [4].

The chopper stabilization technique essentially uses an ac carrier to perform amplitude modulation on the input signal. A chopper stabilized amplifier system consists of modulating and demodulating carriers with period $T = 1/f_{\text{chop}}$, where $f_{\text{chop}}$ is the *chopper frequency*. It should be noted that the signal is bandlimited to half of the chopper frequency to prevent aliasing. Figure 2 displays the relationship between noise and frequency. As seen, the $1/f$ noise is dominant at low frequencies, and thus the low amplitude EEG signals are susceptible to noise from the CMOS transistors. Basically, amplitude modulation using a carrier transposes the signal to higher frequencies where there is no $1/f$ noise, and then the modulated signal is demodulated.
back to the baseband after amplification. A low pass filter with a cut off frequency slightly above the input signal bandwidth ($>f_{\text{chop}}/2$) is used to recover the original signal in the amplified form. Noise and offset are modulated only once, and from the Power Spectral Density Equation, it can be seen that they will be translated to the odd harmonic frequencies of the modulating signal, leaving the chopper amplifier without any offset or low-frequency noise [4].

Therefore, designing the analog front-end is extremely crucial for these applications. In order to achieve the best signal extraction, a front-end with high CMRR, low-noise, and high-pass filter characteristics is required, with configurable gain and filter considerations. Hence this work describes a complete EEG acquisition ASIC with low power dissipation. This paper introduces a novel method by having a fully differential chopper stabilized micro power operational amplifier designed with a negative feedback that behaves like an inherent low pass filter, followed by a fully differential 10-bit successive approximation register ADC. The structure of the paper is as follows. Section II details the padframe and the pin assignments. Section III gives an overview of the test-setup and measurement results and observations.
Chapter 2

Padframe Details and Pictures

2.1 Pin Description

The figure below gives the pin description for the chip.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Padnc</td>
<td>21</td>
<td>$V_{im}$</td>
</tr>
<tr>
<td>2</td>
<td>Padnc</td>
<td>22</td>
<td>$V_{ip}$</td>
</tr>
<tr>
<td>3</td>
<td>Padnc</td>
<td>23</td>
<td>phi1</td>
</tr>
<tr>
<td>4</td>
<td>Ground</td>
<td>24</td>
<td>Reset Global</td>
</tr>
<tr>
<td>5</td>
<td>Digital $V_{dd}$</td>
<td>25</td>
<td>ExtClk</td>
</tr>
<tr>
<td>6</td>
<td>Padnc</td>
<td>26</td>
<td>Bit9</td>
</tr>
<tr>
<td>7</td>
<td>$-V_{dd}$</td>
<td>27</td>
<td>Bit8</td>
</tr>
<tr>
<td>8</td>
<td>Clk3</td>
<td>28</td>
<td>Bit7</td>
</tr>
<tr>
<td>9</td>
<td>Clk2</td>
<td>29</td>
<td>Bit6</td>
</tr>
<tr>
<td>10</td>
<td>Clk1</td>
<td>30</td>
<td>Bit5</td>
</tr>
<tr>
<td>11</td>
<td>Clk0</td>
<td>31</td>
<td>Bit4</td>
</tr>
<tr>
<td>12</td>
<td>I0</td>
<td>32</td>
<td>Bit3</td>
</tr>
<tr>
<td>13</td>
<td>I1</td>
<td>33</td>
<td>Bit2</td>
</tr>
<tr>
<td>14</td>
<td>I2</td>
<td>34</td>
<td>Bit1</td>
</tr>
<tr>
<td>15</td>
<td>I3</td>
<td>35</td>
<td>Bit0</td>
</tr>
<tr>
<td>16</td>
<td>I4</td>
<td>36</td>
<td>Padnc</td>
</tr>
<tr>
<td>17</td>
<td>$V_{ref}$</td>
<td>37</td>
<td>Padnc</td>
</tr>
<tr>
<td>18</td>
<td>$V_{dd}$</td>
<td>38</td>
<td>Padnc</td>
</tr>
<tr>
<td>19</td>
<td>Clk Chopper</td>
<td>39</td>
<td>Padnc</td>
</tr>
<tr>
<td>20</td>
<td>Clkbar Chopper</td>
<td>40</td>
<td>Padnc</td>
</tr>
</tbody>
</table>

The final padframe image is shown in figure 2.2.
2.2 X-Ray Images

A few X-ray images were taken to verify the wire-bonding on the chip, before we started the testing. The following figures illustrate the X-ray
image results. There were no wire-bonding issues observed.

Figure 2.3: X-Ray Image 1.

Figure 2.4: X-Ray Image 2.
Figure 2.5: X-Ray Image 3.

Figure 2.6: X-Ray Image 4.
Figure 2.7: X-Ray Image 5.
Chapter 3

Observations and Measurements

3.1 Setup

The chip was tested after tapeout. The figure (3.1) below shows the test measurement setup. We implemented a detailed setup process, as follows: 1) Testing the Power Supplies and Ground Connections 2) Testing the Output from the Bandgap Reference Circuit 3) Testing the Output from the Analog Front-End 4) Testing the Output pins of the ADC

In the figure below, it is seen that the chip was placed on a protoboard, to avoid any soldering issues. This chip was solely used to test the power supply and ground connections.

Figure 3.1: Test Setup.

Figure 3.2 shows the entire setup, along with the function generators,
DMM, and oscilloscope. For each connection, we observed the current drawn from the supply, and the output in the oscilloscope. For the first stage, we only tested the supplies and the analog front-end.

![Figure 3.2: Detailed Test Setup.](image)

### 3.2 Measurement Results

It was observed that once the analog $V_{dd}$ and ground pins were connected using the power supply, the current drawn was in the order of mA. This does not match the simulated results, where the total current did not exceed 120 $\mu$A. Once the analog $V_{dd}$ and ground were connected, we observed the following:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>$V_{dd}$</td>
<td>3.3</td>
</tr>
<tr>
<td>7</td>
<td>$-V_{dd}$</td>
<td>3.3</td>
</tr>
<tr>
<td>8</td>
<td>Clk3</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>Clk2</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>Clk1</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>Clk0</td>
<td>0</td>
</tr>
<tr>
<td>12</td>
<td>I0</td>
<td>0</td>
</tr>
<tr>
<td>13</td>
<td>I1</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>I2</td>
<td>0</td>
</tr>
<tr>
<td>15</td>
<td>I3</td>
<td>0</td>
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<tr>
<td>21</td>
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<tr>
<td>22</td>
<td>$V_{ip}$</td>
<td>2.238</td>
</tr>
<tr>
<td>23</td>
<td>phi1</td>
<td>3.3</td>
</tr>
</tbody>
</table>
It was important to analyze the source of this large current. The BGR output was zero, and it was observed that there was an open circuit. Therefore, we forced a voltage of 1.65 V at the BGR pin, and checked the current drawn, and it was still in the mA range.

After further analysis of the layout, we discovered that we had shorted the analog, and digital V$_{dd}$, as well as the plus and minus V$_{dd}$. This error was at the padframe level, where we connected the power supplies to the padvdd, and hence there was a short.

This project a great learning experience, and we are grateful to our Professor Dr. Ghovaloo, Mehdi Kiani and MOSIS. The project gave us a sound understanding of analog systems - from a chip design, layout, testing and verification standpoint. We are in the process of analyzing the chip further, and will report any new findings in the near future.
Bibliography


