A Low-Power CMOS Chopper Amplifier for EEG Acquisition Systems

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I. INTRODUCTION

The demand for technologies that help neuroscientists and clinicians to actively observe a large number of neurons in the brain has increased significantly. Currently, the biopotential acquisition systems are bulky and not portable that makes it difficult for the on-going diagnostics and causes discomfort to the patient. There is a need to make these systems more compact and to extend their applications to various fields.

Commonly monitored biopotential signals are EEG, ECG, and EMG. Figure 1 shows the characteristics of these signals, and it can be seen that they have a very low signal amplitude and operate at extremely low frequencies (<150 Hz). This is a major reason their performance is limited by the offset and the noise of the input amplifiers. The physical origin of low frequency noise in MOSFET’s is the carrier number fluctuation theory, or the trapping-detraping model. It is caused by the fluctuation of the number of inversion layer carriers as they are trapped and detrapped to and from traps located in the oxide, and it accounts for the carrier number and the mobility fluctuations [1]. It should also be noted that the typical offset voltages for these applications is around 10 µV.

Some techniques that can be employed to remove the offset and the 1/f noise dynamically include chopper stabilization, autozeroing (AZ), and correlated double sampling (CDS). While the latter two mentioned are sampling techniques, chopper stabilization is a modulation technique that can eliminate the effects of op-amp imperfections. The chopper stabilization technique was first introduced in 1948 by E.A. Goldberg [2]. Earlier, the chopping techniques involved switched ac coupling of the input signal and demodulation of this signal back to the dc signal. While these amplifiers achieved very low offset, and very high gain, they had limited bandwidth and required filtering to remove the large ripple voltages generated by chopping. This problem was solved by introducing the chopper stabilized amplifiers that combined the chopper amplifier with a conventional wideband amplifier that remained in the signal path [3]. The chopper stabilization technique essentially uses an ac carrier to perform amplitude modulation on the input signal. The principle of chopper amplification is demonstrated in figure 2 [4]. As seen in the figure, the system consists of modulating and demodulating carriers with period T = 1/f_{chop}, where f_{chop} is the chopper frequency. It should be noted that the signal is bandlimited to half of the chopper frequency to prevent aliasing. Basically, amplitude modulation using a carrier transposes the signal to higher frequencies where there is no 1/f noise, and then the modulated signal is demodulated back to the baseband after amplification. A low pass filter with a cut off frequency slightly above the input signal bandwidth (>f_{chop}/2) is used to recover the original signal in the amplified form. Noise and offset are modulated only once, and from the Power Spectral Density Equation, it can be seen that they will be translated to the odd harmonic frequencies of the modulating signal, leaving the chopper amplifier without any offset or low-frequency noise [4].

II. DESIGN DETAILS

A. DC Offset Zeroing Technique

Since the EEG signals operate at extremely low voltage range, they are associated with high common-mode interferences. There is also a significant differential electrode offset (DEO) voltage created between the biopotential electrodes just before amplification. Many techniques have been proposed in [5] [6]. This paper will focus on using the DC Servo Loop outside the choppers that will introduce a high pass filter mechanism. The circuit is shown in figure 3. It is divided into a coarse low pass filter with discrete cut levels and a fine low pass filter with a continuous output range [7].
B. Chopping and Filtering Technique

The principle of this technique was discussed in section I. The input signal is modulated to the chopping frequency, amplified and then demodulated back to the baseband. Typically, the offset from the amplifier is modulated only once and appears at the chopping frequency and its odd harmonics.

The residual offset of a chopper amplifier exists and typically is in the order of µV. Basically the residual offset of a chopper amplifier mainly arises from the spikes of the input chopper, or from the charge injection mismatch of the switches. A major reason this arises is due to the input impedance $R_{in}$ and the mismatch in parasitic capacitive coupling between the chopping signal and the input lines. A technique to solve this problem is using nested choppers. The idea is to consider the conventional chopper as a regular amplifier with no 1/f noise and a reduced offset. This offset can be reduced by applying another pair of choppers that now operate at a much lower frequency. Because this chopper works in a low frequency, the residual offset is reduced even further. However, it would be hard to implement this technique, since the usage of two amplifiers shoots up the power dissipation, which is one of the most critical specification.

After demodulation, the system normally consists of a low pass filter, that will eliminate high frequencies in which the offset and the noise were present. The technique for low pass filtering discussed in this paper consists of a pole configuration 2-stage amplifier. A dominant pole is placed at the second stage and a second pole is placed at the first stage. In order to meet the stability requirements, the cutoff frequency of the first stage will be designed to a higher frequency when compared to the gain crossover frequency of the amplifier. As seen in figure 4, the cutoff frequency of the second stage can be designed lower than the $f_{chop}$. The phase compensation capacitor will work as a narrow band first-order LPF which will satisfy the filtering requirements [4]. The equation for the input referred noise of this amplifier will be

$$V_{n,in} = V_{th1} + V_{fn2} + V_{tn2} / A_1$$

In the equation $V_{th1}$ and $V_{tn2}$ are the thermal noise of the first two stages, $V_{fn2}$ is the noise of the second stage and $A_1$ is the first stage gain.

III. BLOCK DIAGRAM AND DESIGN SPECIFICATIONS

The figure below is the overall block diagram of the system that was discussed in detail in the previous section. Following the block diagram is a chart specifying our design specifications. As seen in the figure, the HPF is used to zero the DC offset, and the method proposed is using the DC servo-loop outside the choppers. The next block is the chopper amplifier block - and the proposed method is using a 2-stage amplifier after the demodulator - that not only improves the stability, increases gain, but also acts as a low pass filter to get rid of the higher frequencies containing the residual offset and the 1/f noise.

![Block diagram of the system](image)
IV. APPENDIX

A. Comparison Chart

The table here shows the advances made by different groups.

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<tr>
<td>Supply Voltage</td>
<td>3V</td>
<td>3V</td>
<td>1.8V</td>
<td>3V</td>
<td></td>
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<td>Current Consumption</td>
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<td>11.4µA</td>
<td>1.26µA</td>
<td>2.5µA</td>
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<td>Input Referred Noise (0.1-30Hz)</td>
<td>0.57µV/√Hz (V/√Hz)</td>
<td>0.97µV/√Hz (V/√Hz)</td>
<td>0.93µV/√Hz (V/√Hz)</td>
<td>0.57µV/√Hz (V/√Hz)</td>
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<td>CMRR</td>
<td>&gt;110dB</td>
<td>&gt;80dB</td>
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<td>105dB</td>
<td>&gt;128dB</td>
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<td>Input Impedance</td>
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<td>&gt;100KΩ</td>
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<td>BPF 3-dB cut-off frequency</td>
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<td>0.31Hz</td>
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<td>0.11Hz</td>
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<td>50mV</td>
<td>45mV</td>
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<td>0.41mm²</td>
<td>1.4mm²</td>
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<td>9.2</td>
<td>9.9</td>
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Fig. 7. Comparison chart [4]

References for this chart: