Switched-Capacitor Charging System for an Implantable Neurological Stimulator

Draft 1

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I. INTRODUCTION

Integrated medical stimulators have been around for almost six decades, beginning with the development of the cardiac pacemaker and gaining momentum with the miniaturization of integrated circuit technologies. Year by year, researchers strive to make such devices smaller, more accurate, and more capable while consuming less power. Hence, wireless power and efficient stimulation techniques have been popular topics of research. The goal of this design is to focus on the latter.

Typically, neural stimulation is accomplished via voltage controlled stimulation (VCS) or current controlled stimulation (CCS). While VCS has proved to be very efficient, complex safety measures must be implemented to avoid tissue damage. Conversely, CCS is much safer, but boasts a much lower efficiency. However, work has been done on the development of a third technique, named switched-capacitor stimulation (SCS), which uses a capacitor bank to store charge and stimulate tissue [1,2]. By utilizing efficient capacitor charging techniques [3], an SCS device could provide high power efficiency with minimal safety overhead. Below, Figure 1 exhibits a block diagram of our design. Note that the elements outside of the box are inputs and outputs of the system.

II. SYSTEM ARCHITECTURE

Active-Rectifier: This is previously designed high-efficiency rectifier [4,5], which provides the supply voltages (VDD and VSS) for both the analog and digital components of the system. The reason for excluding this block in our design flow is it’s large IC area consumption in addition to the required area for the rest of the system.

Digital Control: This controls the switching signals of the multiplexers (SA, SB, SC), as well as providing an 8-bit number to the DAC (DACin). The digital controller has two inputs: CFull and Q_int. CFull indicates that a capacitor is fully charged so that the controller can switch and charge another capacitor. Q_int is a voltage that can be integrated to determine the charge balance of the stimulation. Since this signal is an analog voltage, an ADC will be required so that an adequate corrective processing can be done inside the controller.

Digital to Analog Converter (DAC): The DAC receives an 8-bit input which specifies the value of an analog voltage to be used as a reference for either the driving circuit of the AC-DC converter or the comparator. This analog voltage can be anywhere in between VSS and VDD; to maintain a sufficient resolution, given by

\[ \frac{V_{DD} + |V_{SS}|}{2^N} \]

where N is the number of input bits, a resolution of 8 bits was selected to achieve fine tuning of the reference given some charge imbalance. Also, this feedback loop ought be faster than the capacitor charging in order to effectively compensate the imbalance. Therefore, the speed of the DAC should be greater than 5kHz for the largest allowable charging time.

Figure 1. Switched-capacitor stimulator system diagram.
Comparator and Monostable: The voltage comparator is a part of the discharge control loop of the capacitors. Its job is to compare the voltage of each one of the stimulation capacitors with the reference voltage and trigger a signal whenever these two voltages are equal. This process allows the digital controller to know when to switch and charge an empty capacitor. The monostable allows the control signal to stay active for a certain period of time to ensure it is latched by the digital control. As a safety measure, a watchdog timer is included to trigger the monostable in case the capacitor’s voltage never reaches $V_{REF}$. There are no critical performance criteria for these blocks.

AC-DC Converter and Driving Circuitry: These functional blocks are responsible for efficiently converting the AC input signal, which comes from the inductive link, into a DC voltage to be stored in the stimulation capacitors. A general diagram of a tentative topology is shown in figure 2. The driving circuitry will consist of a control loop that will regulate the switch voltages, thereby controlling the charging profile of the load capacitors. Accuracy of the driving circuitry will greatly determine charging efficiency. In terms of performance, this block must be able to operate in the MHz range, be able to charge two complementary capacitors with 1.8uC in less than 1.25ms, and boast an efficiency of at least 60% [6].

Figure 2. AC-DC capacitor charging scheme.

Multiplexers: A series of multiplexers, controlled by the digital controller, will serve as bridges between the capacitor bank and, either, the output of the AC-DC converter or the stimulation electrodes. Ideally, switch resistances should be as low as possible to reduce power loss, but this will be a trade-off with area.

Charge Balance Circuit: The charge balance circuit is composed of a voltage-controlled resistor, which generates a voltage proportional to the return current from the stimulation site. An integrator will integrate the generated voltage over a biphasic stimulation period. Depending on the polarity and magnitude of the output, the digital controller will adjust $V_{REF}$ to compensate. Currently, it is not intended to implement the integrator on-chip; however, if space and time allow, this could be accomplished. The accuracy of the integrator will determine the effectiveness of the charge balance system; therefore, it must be very accurate and robust.

Support Blocks: A voltage reference generator will be needed to provide a reference for the DAC to generate its voltages. A clock generator will be used as the timing reference for all the clocked signals in the system. These blocks are not shown in the diagram because they serve as support blocks to the rest of the components in the IC.

III. CONCLUSION

This design will be divided into two main portions. Orlando and Jose will head the development of the AC-DC converter and its supporting components. Diego and Divyanshu will lead the development of the DAC and its related blocks. Other blocks will be divided among the members according to the progress made in each area. Due to the limited size and number of pads, it was decided to implement a minimal proof of concept design, which could be readily expanded. Additionally, a few performance parameters have been mentioned, but many still remain to be determined. Overall, low power consumption and high frequency operation govern each block.
IV. REFERENCES


