Draft 2: A Low Power CMOS Chopper Amplifier
for EEG Acquisition Systems

S. Devarakond, B. Narayan, H. Sane, J. Zaveri

March 4, 2009
Contents

1 Introduction 2

2 Components of the System 4
  2.1 Electrode-Tissue Interface ................................. 4
  2.2 High Pass Filter ........................................... 5
  2.3 Analog Multiplexer ........................................... 5
  2.4 Chopper Modulator and Demodulator .......................... 6
  2.5 Fully Differential Folded Cascode Amplifier .................... 7
  2.6 Analog-Digital Converter ..................................... 9
    2.6.1 ADC blocks ........................................... 9

3 System Integration 11

Bibliography 14

A SIMULINK pictures 16

B AMI 0.35 µ Process Models 18
Chapter 1

Introduction

The demand for technologies that help neuroscientists and clinicians to actively observe a large number of neurons in the brain has increased significantly. Currently the biopotential acquisition systems are bulky and not portable that makes it difficult for the on-going diagnostics and causes discomfort to the patient. There is a need to make these systems more compact and to extend their applications to various fields.

Commonly monitored biopotential signals are EEG, ECG, and EMG. Figure 1 shows the characteristics of these signals, and it can be seen that they have a very low signal amplitude and operate at extremely low frequencies (<150 Hz). This is a major reason their performance is limited by the offset and the noise of the input amplifiers. The physical origin of low frequency noise in MOSFETs is the carrier number fluctuation theory, or the trapping-detrapping model. It is caused by the fluctuation of the number of inversion layer carriers as they are trapped and detrapped to and from traps located in the oxide, and it accounts for the carrier number and the mobility fluctuations [1]. It should also be noted that the typical offset voltages for these applications is around 10 µV.

As discussed in draft-1, EEG waves are common biopotential signals that are recorded frequently in modern clinical practise. Due to the low frequency and µV level amplitude of these signals, they are often dominated by noise. Also present are the common-mode interference from the mains, as well as electrode-offset. Therefore, designing the analog readout front-end is extremely crucial for these applications. In order to achieve the best signal extraction, a front-end with high CMRR, low-noise, and high-pass filter characteristics is required. The front-end should also have configurable gain and filter considerations.

The block diagram discussed in draft-1 is shown in the figure below.

The figure above is the overall block diagram of the system that was discussed in detail in the previous section. Each block will be discussed in detail in the coming sections. The input channels consist of the signals
obtained by the electrodes. The DC offset caused due to the metal electrodes can be cancelled by the high pass filter. Analog multiplexer determines the input signal that is fed into the chopper stabilized instrumentation amplifier. They are then modulated to higher frequencies, such that the even harmonics contain the signals, and the odd harmonics the noise. After amplification, these signals are demodulated and are passed through a low pass filter - to get rid of the noise present at the lower frequencies, and finally fed into the Analog-Digital Converter.

The table below lists the specifications of the project (obtained from draft-1).

<table>
<thead>
<tr>
<th>Design Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Process</td>
</tr>
<tr>
<td>Supply Voltage</td>
</tr>
<tr>
<td>Chopping Frequency</td>
</tr>
<tr>
<td>Gain</td>
</tr>
<tr>
<td>CMRR</td>
</tr>
<tr>
<td>PSRR</td>
</tr>
<tr>
<td>Power Dissipation</td>
</tr>
<tr>
<td>LPF cutoff frequency</td>
</tr>
<tr>
<td>Noise (input referred)</td>
</tr>
<tr>
<td>Functional Range</td>
</tr>
</tbody>
</table>
Chapter 2

Components of the System

The various blocks from the system are explained in detail in this section.

2.1 Electrode-Tissue Interface

The electrode-tissue interface plays an important role in determining the inputs to the amplifier. It is essentially a series RC circuit, and affects the inputs if the series capacitance would create a high-pass pole for the signal chain. To overcome this, it is important to choose a large impedance, which would ensure that the high pass pole is determined by the on-chip circuitry. After a thorough analysis of the electrodes choice, we propose using Platinum-iridium electrodes. As described in [2], PtIr is a polarizable material, and it forms a double-layer junction with an excess capacitance from the plating of ions. As seen in the figure below, it is an equivalent 3.2 $\mu$F capacitor in series with a 1kohm resistor. The paper also shows that the dc headroom for the diagnostic recording system is around 15 mV. The area occupied by these electrodes is around 6mm$^2$.

The series RC model of the interface is given in the figure below.

![Series RC circuit](image.png)

Figure 2.1: Series RC circuit: Offset due to electrodes.

The differential DC voltage between the biopotential electrodes is of the order of 10-50 mV. It is important to eliminate this offset before the signal reaches the amplifier. Rejection of the electrode dc offset before amplification is a must in order to achieve the required dynamic range. The method
we propose is using a High Pass Filter technique with a very small corner frequency (0.5 Hz).

2.2 High Pass Filter

As mentioned above, to reduce the required capacitance for a high pass corner frequency of below 0.5 Hz, a very large resistance is needed. And this high pass filtering should take place before the signal is upconverted. We also must keep the flicker noise to a minimum level, and hence no active devices are used in this block [3]. The resistor is obtained from the switched-capacitor circuit, as seen in the figure. The equivalent filter resistance, $R_f$ is given by:

$$ R_f = \frac{T_c}{2C_{in}} $$

![Figure 2.2: High pass filter to minimize DC offset.](image)

2.3 Analog Multiplexer

The advantage of an analog multiplexer is that it allows the use of a single amplifier to service multiple recording sites. The details of a typical 4-channel analog multiplexer is shown in figure below [4]. The input signals are INO-IN3 and the select signals are S0-S3. The multiplexer consists of NMOS transmission gates that basically pass the signal when their gates turn on, and are high impedance when the gates are turned off. With this topology, there can be charge injection and clock feedthrough. These issues can be eliminated using dummy switches, as shown in the figure. The dummy switches are also inserted between the recording sites and main switches to reduce the effect of charge feed-through from the neural signal[4].
2.4 Chopper Modulator and Demodulator

The chopper stabilization technique essentially uses an ac carrier to perform amplitude modulation on the input signal. The principle of chopper amplification is demonstrated in figure 2.4 [4]. As seen in the figure, the system consists of modulating and demodulating carriers with period $T=1/f_{\text{chop}}$, where $f_{\text{chop}}$ is the chopper frequency. It should be noted that the signal is bandlimited to half of the chopper frequency to prevent aliasing. Basically, amplitude modulation using a carrier transposes the signal to higher frequencies where there is no 1/f noise, and then the modulated signal is demodulated back to the baseband after amplification. A low pass filter with a cut off frequency slightly above the input signal bandwidth ($>f_{\text{chop}}/2$) is used to recover the original signal in the amplified form. Noise and offset are modulated only once, and from the Power Spectral Density Equation, it can be seen that they will be translated to the odd harmonic frequencies of the modulating signal, leaving the chopper amplifier without any offset or low-frequency noise [4].
below. When the CLOCK is low, the modulator inverts the signal, and does not invert the signal when CLOCK is high. The residual offset of a chopper amplifier exists and typically is in the order of $\mu$V. Basically the residual offset of a chopper amplifier mainly arises from the spikes of the input chopper, or from the charge injection mismatch of the switches. A major reason this arises is due to the input impedance $R_{in}$ and the mismatch in parasitic capacitive coupling between the chopping signal and the input lines. A technique to solve this problem is using nested choppers [8]. The idea is to consider the conventional chopper as a regular amplifier with no 1/f noise and a reduced offset. This offset can be reduced by applying another pair of choppers that now operate at a much lower frequency. Because this chopper works in a low frequency, the residual offset is reduced even further. Figure 2.5 demonstrates this. The conventional chopper is considered as a regular amplifier without the 1/f noise and a reduced offset. The offset of this amplifier can be reduced by applying another pair of choppers, which operate at a much lower frequency, as the 1/f noise is already removed. As the outer pair is working at a much lower frequency the residual offset due to spikes of these choppers is reduced greatly. The spikes that are generated by the high chopping frequency are modulated by the output chopper with a lower frequency.

Figure 2.5: Circuit to implement chopper modulator/demodulator.

Figure 2.6: Nested chopper technique to minimize the spike.

2.5 Fully Differential Folded Cascode Amplifier

The proposed op-amp topology is shown in figure 2.7 [6]. It is essentially a fully differential folded cascode structure, since this structure has a better
noise performance [7]. In addition, the structure also has two miller compensated capacitors, as seen in the figure. The differential input pair is based on P-channel devices. The load consists of four cross-coupled transistors, and it presents a low impedance for common mode signals, and for differential signals this load can be high. This in-turn provides a high common-mode rejection ratio. The minimum power supply voltage is given by:

\[ V_{DD} = V_{thp} + 3V_{DS, sat} \]

Figure 2.7: Fully differential folded cascode with miller compensation.

Since the first stage has a high CMRR, the common-mode feedback can only be applied to the second stage. The topology we propose consists of a switched-capacitor circuit for the CMFB. A folded cascode structure was preferred in order to keep the power supply voltage as low as in the main fully differential opamp. As seen from the figure, during the inactive clock phase, \( C_3 \) and \( C_4 \) are precharged up to \( V_{DD} \), and \( C_5 \) is discharged. During the active phase of the opamp, the negative feedback holds the voltage in the positive input of the CMFB close to ground. \( C_5 \) is now connected to the supply, \( V_{DD} \). We can determine the charge balance equation by:

\[ (V_{pout} - V_{DD})C_3 + (V_{nout} - V_{DD})C_4 + (V_{DD} - V_{SS})C_5 = 0 \]

Figure 2.8: Circuit to implement chopper modulator/demodulator.

This topology was implemented in Cadence, as seen in the figure below. We are still working on the stability and power consumption of the circuit.
Figure 2.9: Cadence implementation of the opamp discussed above.

However, preliminary results show an open loop gain of 80 dB. The op-amp is designed for a total power consumption in the range of 90 $\mu$W (power supply voltage of 1.8 V was assumed).

### 2.6 Analog-Digital Converter

The chopper stabilized amplifier provides analog EEG signal after removing noise signal. This signal is then converted to digital form using ADC. Flash ADCs and pipelined ADCs provide fast conversion. However, they have high power dissipation, and consume large amount of area. Oversampling ADCs such as sigma-delta provide high precision but cause delay.

For this application, successive approximation ADC (SAR ADC) provides sufficient accuracy along with good speed. It also gives very low values for power dissipation, and chip area; both critical issues for this application.

Analog input is given through sample-and-hold circuit to a comparator. Final digital output is passed through a DAC and given as second input to comparator. Comparator gives high or low decision. Comparator output is given to SAR logic block which assigns logic value to each bit of digital output. It needs a clock cycle for every bit of resolution of the digital output.

#### 2.6.1 ADC blocks

As seen in the figure, the different blocks of the ADC are discussed below:

**Sample-and-hold circuit:** Amplifier output is passed through sample-and-hold circuit before giving to comparator. We plan to use switched-capacitor circuit for this purpose.

**Comparator:** Amplifier output is given to positive input by sample-and-hold circuit. DAC output is connected to negative input. If DAC output
is greater than amplifier output, comparator gives logic 0 signal; and vice versa.

**SAR register**: It consists of an N-bit shift register, followed by a combinational circuit. It operates on an externally given clock input. In 1st cycle, its sets MSB bit and resets all other bits. If comparator output = 1, then it keeps MSB bit as 1, else resets it. In next clock cycle, it sets the bit next to MSB. Thus, after N clock cycles, the register contains the digital value of amplifier output. SAR register then writes the register value into output register and gives it a "done" strobe command.

**Output register**: It is an N-bit register. When it receives "done" strobe from SAR register, it assumes it contains valid data which it proceeds to send to block connected at its output.

**DAC**: We plan to use a capacitive conversion network as a DAC. It consists of a capacitor and a switch for every bit of resolution. So for 8-bit resolution, we have 8 capacitors and 8 switches. One plate of each capacitor is connected to the negative input of the comparator. 2\textsuperscript{nd} plate of each capacitor is connected to a switch. Logical value of each switch is determined by SAR register value. Capacitor values are in decreasing order from MSB to LSB. If total capacitance = C, then MSB capacitor value = C/2\textsuperscript{1}, next cap value = C/2\textsuperscript{2} and so on. LSB cap value = C/2\textsuperscript{8}. The relation is \( C_n = C_0 2^n \) where \( C_0 \) is unit capacitor (LSB). A 9\textsuperscript{th} capacitor is connected with value = C/2\textsuperscript{8} so that total capacitance value except MSB cap is equal to C/2\textsuperscript{1}. Its role is to terminate the capacitor array so that total capacitance achieves desired value of \( C_t = C_0 2^N \) where N is resolution of the ADC.

**Specifications**: We plan to use an 8-bit ADC. From literature study, this type of ADC for 8-bit resolution dissipates power in the range of 50 \( \mu \)W to 120 \( \mu \)W [8].
Chapter 3

System Integration

All the blocks mentioned above were integrated into a system - and simulations were performed in SIMULINK. The figure below gives the overall system that was built in SIMULINK.

Shown in the figure is the simulink model for each of the blocks of our system. The electrodes are modeled using their equivalent parasitic resistance of 100 Ω and capacitance 3.2 µF. EEG input from the electrodes is given to a low pass filter with a $f_{-3dB}$ frequency of 0.5 Hz to remove the DC offset (40mV). The signal is frequency upconverted using a modulator with 4 kHz clock. The noise involved due to the switch capacitors circuits used in the HPF as well as the modulator is added at this point. This signal is now amplified using an amplifier system with gain 80 dB. In our system we will be using a differential opamp configuration for amplification. However during modeling we used a single ended opamp for simplicity. We also model the opamp noise using an equivalent model to include the 1/f noise, thermal noise and DC offset noise [10]. The signal is now down-converted using a demodulator and the signal is given to a low pass filter having a $f_{-3dB}$ of 2 kHz. Finally the analog output is converted to a digital output using a successive approximation type ADC. The quantization noise and the capacitive noise are further added at the output of the idealized ADC quantizer.

After each stage, the output was seen through the "scope" function. Following is a list of plots we observed while building the entire system after each block. (clearer pictures in Appendix 1).
Figure 3.1: Simulink model of entire ASIC with non-linearities included.
Figure 3.2: Input with DC Offset.

Figure 3.3: EEG input after HPF and no DC offset.

Figure 3.4: Output from Modulator.

Figure 3.5: Output from the amplifier.

Figure 3.6: Output from the demodulator.

Figure 3.7: ADC output.
Bibliography


Appendix A

SIMULINK pictures

After each stage, the output was seen through the "scope" function. Following is a list of plots we observed while building the entire system after each block - a clearer bigger picture. (same as section 3).

Figure A.1: Input with DC Offset.

Figure A.2: EEG input after HPF and no DC offset.
Figure A.3: Output from Modulator.

Figure A.4: Output from the amplifier.

Figure A.5: Output from the demodulator.

Figure A.6: ADC output.
Appendix B

AMI 0.35 $\mu$ Process Models

We characterized the basic nmos ($W/L = 1\mu/0.7\mu$) and pmos model ($W/L = 2\mu/0.7\mu$)

The following characteristics helped us verify the parameters in the model file with the simulations results.

Figure B.1: Id versus Vgs plot - extraction of Vthp.
Figure B.2: Id versus drain-source plot.

Figure B.3: Id versus Vgs plot - extraction of Vthn.

Figure B.4: Id versus drain-source plot.