Georgia Institute of Technology  
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING  
ECE 6414: Analog Integrated System Design – Spring 2009  
11:00am – 12:00 pm, Mon, Wed, Fri, Klaus 2443  
http://www.ece.gatech.edu/academic/courses/ece6414/S09  

Instructor: Maysam Ghovanloo, Ph.D. (mghovan@ece.gatech.edu), Phone: (404) 385-7048  
Office Hours: Fridays 2:00-4:00 pm, other times with prior appointment  
TA: N/A  

Textbooks:  

Other References: (recommended)  
1. Analysis and Design of Analog Integrated Circuits  
   P. Gray & Meyer  
2. Design of Analog CMOS Integrated Circuits  
   B. Razavi  
3. The Art of Analog Layout  
   A. Hastings  
4. Analog Integrated Circuit Design  
   D.A. Johns and K. Martin  

Prerequisites: Analog Electronics (ECE-4430 and 3050 or equivalent), Co-requisites: None  

It is assumed that you are familiar with the following topics:  
1. Circuit theory, frequency response, small signal analysis.  
2. Solid-state devices and microelectronic circuits: P-type and N-type semiconductors, diodes, bipolar junction transistors, and MOS field-effect transistors (MOSFET).  
3. Analog circuit building blocks such as current mirrors, reference generators, single stage and differential amplifiers, and OpAmps.  
4. Knowledge of MATLAB and available CAD tools such as SPICE or Cadence.  

Course Description:  
We look at some of the more advanced analog building blocks such as fully-differential OpAmps and dynamic analog circuits. We will use analog IC building blocks to construct simple analog IC systems such as data converters, filters, mixers, etc. We also review the characteristics and specifications of such analog and mixed-mode circuits from the system design perspective. This course is highly design/project oriented and emphasizes on intuitive understanding of circuits, particularly those topics used in analog ASIC design. As such, it can be quite time consuming.
However, it will provide you with precious hands-on experience as you go through a realistic analog ASIC design cycle from scratch to tapeout. Organization, attention to the smallest details, compromise, optimization, time management, and teamwork will also prove to be quite important in analog integrated system design.

**Topical Outline:**

Introduction, Review of basic analog IC building blocks  
Noise analysis in analog circuits  
Advanced current mirrors, amplifiers, and filters  
Switched-capacitor circuits  
Fully differential and high performance OpAmps  
High speed comparators  
Digital-to-analog converters (DAC)  
Analog-to-digital converters (ADC)  
Nonlinear analog circuits and mixers

**Course Project:**

Groups of 2 or 3 students should choose a topic of their interest using some of the major analog and mixed-mode circuit blocks, discussed in this course, in an analog system with application in biomedical engineering. Teams are encouraged to consult with the instructor or other faculty in choosing their topic. Each team proposes their project topic in a 2-page draft by Draft-1 deadline (about 1 month through the semester). Draft-1 should include a rough block diagram of the analog system showing the inputs and outputs of each block, as well as their expected performance ratings. It should include a brief description of the biomedical application and any relevant online or published references that the group might have visited. It should also indicate the role and responsibilities of each team member. Each team should select one of the members as the team leader, who will be the main point of contact with the instructor.

After receiving approval from the instructor, team members perform a thorough literature survey on their selected topic, and come up with an analog ASIC design idea that would serve a specific purpose in the selected application. Depending on its complexity, the project might be defined as part of a larger system. It is also possible for 2 or 3 teams to take on the design of various components of a larger analog system.

A summary of the literature survey, a detailed system block diagram, and selected circuit topologies for each block should be included in a 2nd Draft, and turned in by Draft-2 deadline (about 2 months through the semester). System level simulations using ideal circuit components in Cadence, MATLAB, Simulink, or any other CAD tool is highly encouraged at this stage. Please note that ECE-6414 does not include any CAD tool training. In case you do not have enough prior background, make sure to go through online tutorials and consult with the other team members. The instructor will provide each group with individual feedback on Draft-2.

At this stage, team members start implementing their ASIC designs at the transistor level, including layout, using Cadence tools. All ASIC designs should target AMI-0.5\(\mu\)m standard CMOS processes. Detailed information about this process and transistor models are available through MOSIS website (www.mosis.org). This process operates reliably in 3-5V supply range. Using certain low voltage circuit design techniques, operation at lower voltages is also possible.
Considering the significance of ASIC layout in the performance of analog circuits, important layout design techniques that affect the circuit performance in terms of matching, minimizing parasitic components, and linearity, will be covered in class. The entire proposed circuit/system should be laid out, following these layout design guidelines. Part of the project grade is dedicated to the layout quality and post layout simulations. Your entire layout, including pad frame and protection circuitry should fit within half of a MOSIS “Tiny Chip”, which means 1500um x 750um. Every two teams will be sharing one Tiny Chip.

There will be a Design Review about a month after Draft-2, when all circuit schematics at transistor level should be complete and simulated. The instructor will review the simulation results for each design along with the team members at a computer station and provide them with feedback. Part of the simulation results will be graded at this stage.

The team members will have a chance to modify and improve their circuit designs during the last month of the semester as they layout their designs and observe the performance of their circuit blocks more realistically in post-layout simulations.

All the schematic modifications, simulations, and layouts have to be completed by the last day of classes, which is indicated as the “Tapeout” date on the course schedule. The instructor will hold a second design review on that day and review the layouts and post-layout simulations with the team members. The top-level schematic and layout of the ASIC design should pass design rule check (DRC) and layout vs. schematic (LVS).

Finally by the end of the semester each team will turned in a report that should follow the IEEE standard journal format. This paper should include the complete design, a summary of the literature survey, design theory and calculations, complete circuit schematics, circuit layout, pin-out diagram, post-layout simulation waveforms, testing and measurement procedure (after fabrication), and a summary of circuit characterization results (through post layout simulations). Links to the IEEE general information for authors is provided on the course webpage. There, you can also find template files for MS-Word. The page limit for your final paper is 10 pages. This is the portion of the paper that will be graded based on completeness and quality of writing. However, each team can add an unlimited number of appendixes to fully document their work.

During the final exam, each group should present the entire project in a 15-min slide presentation (~15 slides) for the rest of the class in a conference style. This session will be open to the public audience. Other faculty members and senior graduate students might be invited to evaluate the projects. The entire group should participate in the presentation and will be asked questions for 5-min by the instructor and other audience after their presentation.

To assess the individual participation of the team members, each member of the team will be asked to fill out an individual effort assessment form about the other team members.

Those teams with best functional circuit designs, based on post-layout simulations and other performance measures, will be given a chance to submit their IC layouts to MOSIS for fabrication. The actual tapeout date, according to the MOSIS schedule for AMI-0.5, is going to be either 5/25/09 or 6/22/09.

Group members are encouraged to test and characterize their ICs after fabrication. Functional devices will be considered for additional experiments in their particular biomedical applications. If successful, measurement and experiment results can potentially be considered for submission to professional meetings and even journal publications.
Here are some further important details about the projects:

- You may discuss questions in large groups, but each person must independently perform and answer questions related to the entire project work. Therefore, the grading will not be the same among members of each group.

- For the final presentation you should describe the background for your system (literature search results), state-of-the-art, methods, simulation results, challenges, and solutions. One should use fonts that can be visible when projected. One should keep the number of slides to 20 or less. One should minimize the number of slides with text only (I would strongly prefer no slides with text only, other than a conclusion slide at the end). Results should be word-processed (no hand drawn / hand written materials / none scanned in).

- All project related materials are due electronically by email to me (mgh@gatech.edu) at 10am on the day that they are due. In the e-mail please identify name (of all people in the project), as well as on the first slide, so I know who should get credit for the project. Projects handed in after this deadline and before the beginning of the class on the same day will be graded from 50% of the full grade. After the beginning of the class, no project will be accepted. This policy is firm, so do not fall behind! The work load will not get any lighter later in the semester.

- Only one set of slides will be accepted per team. To help me archive the presentation files, please use this naming convention:

  Team#_Draft1_ECE6414_S09.ppt , Team#_Presentation_ECE6414_S09.ppt , etc.

- Try to add a relevant title for each slide and add a brief description so that your slides would be self explanatory. Also try to add one or two slides at the end as a conclusion.

**Reading Assignments:**

I will not keep track of class attendance. However, you are highly encouraged to attend all class and makeup sessions. Because there might be discussions in class that are not covered in the notes or textbooks.

**Reading Assignments:**

Reading assignments include sections of the textbooks, supplementary notes, literature search, and online articles that are relevant to the course topics. Class notes and supplementary notes, which topics may or may not be included in the textbook, will be posted on the class webpage and it is your responsibility to print them out and bring to the class with you. These materials will not be handed out during lectures. Students are responsible for both lecture material and reading assignments for the midterm, project, and final examinations.

**Homework:**
Homework will be assigned, as seen on the course webpage. The homework will include designs, hand calculations, and computer simulation problems using SPICE. The homework will not be collected, but you are expected and highly encouraged to complete the problems because variations of those problems could be used in the exams.

Exams:

- There will be one evaluation and two closed book midterm examinations each of 60 minute duration.
- Rules of exam: One sheet of notes, last exam's sheet of notes, and a calculator.
- Each exam is basically cumulative: Every unit builds on all the previous units.
- Expect the unexpected: The exam will be over material covered in lectures (primarily), handouts, and in the textbook, but I reserve the right to make any / all problems not look like homework problems. I expect that you get the intuition of the key concepts from the homework. In the exam, you should be able to apply these concepts to slightly different problems.
- All grades become final one week after they are returned in class.

Missed Exam:

If you miss midterm exam or do not attend your project presentation without a certified medical excuse or my prior approval, a zero will be averaged into your grade. Certified excuses and prior approval will be dealt with individually. Generally, only one makeup exam will be held at a designated time near the end of the semester and before the final exam. This means that there will be only one make-up test, independently from which exam/presentation you miss. Thus, the make-up test will be comprehensive. To request an excused absence, 1- write a formal letter to me (typeset), dated and signed, stating your specific request and the reason you are asking for an excused absence; 2- provide documentation supporting your request; 3- bring this letter and the documentation to me in person before the requested date (if an absence is foreseeable) or within one week after the absence (if it is of unforeseeable nature), at which time your request will be discussed. Special cases will be dealt individually.

Academic Integrity:

It is the responsibility of the instructor to encourage an environment where you can learn and your accomplishments will be rewarded fairly. Any behavior which compromises the basic rules of academic honesty as described in the General Catalog will not be tolerated. It is the instructor’s understanding that the student’s signature on any test or assignment means that the student neither gave nor received unauthorized aid. For more information: http://www.deanofstudents.gatech.edu/integrity/

Disabilities:

Reasonable accommodations will be made for students with verifiable disabilities. To qualify for these accommodations, students must register with Access Disabled Assistance Program for Tech Students (ADAPTS). For more information: http://www.adapts.gatech.edu/

Grading Policy:
Evaluation Exam  5%     A: 90 – 100
Midterm-1     15%     B: 70 – 89
Midterm-2     20%     C: 50 – 69
Project       60%     D: 40 – 49
                F: 0 – 39

Project Grading:        Draft-1    5%
                        Draft-2     10%
                        Layout quality/techniques 10%
                        Simulation results     10%
                        Circuit performance    10%
                        Presentation          25%
                        Final Paper           25%
                        Group cooperation    5%

Auditing Criteria:
The ECE department does not grant any auditing credit. However, if you are interested in just sitting in the class, please contact me.

Course Schedule (Tentative):

<table>
<thead>
<tr>
<th>Exam/Project</th>
<th>Date</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Evaluation Exam</td>
<td>Friday 1/30/09</td>
<td>In class</td>
</tr>
<tr>
<td>Project Draft 1</td>
<td>Friday 2/6/09</td>
<td>10 am</td>
</tr>
<tr>
<td>Midterm 1</td>
<td>Friday 2/20/09</td>
<td>In class</td>
</tr>
<tr>
<td>Project Draft 2</td>
<td>Monday 3/2/09</td>
<td>10 am</td>
</tr>
<tr>
<td>Design Review</td>
<td>Monday 3/27/09</td>
<td>4-6 pm</td>
</tr>
<tr>
<td>Midterm 2</td>
<td>Friday 4/3/09</td>
<td>In class</td>
</tr>
<tr>
<td>Tapeout</td>
<td>Friday 4/24/09</td>
<td>4-6 pm</td>
</tr>
<tr>
<td>Final Presentations</td>
<td>Monday 4/27/09</td>
<td>2:50 - 5:40pm</td>
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<tr>
<td>Final Papers</td>
<td>Wednesday 4/29/09</td>
<td>10 am</td>
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Notes: