LECTURE 440 – SIMPLE MOSFET OP AMPS
(READING: Text-Sec. 6.4 and 6.8)

INTRODUCTION
The objective of this presentation is:
1.) Illustrate the analysis of MOS op amps
2.) Prepare for the design of MOS op amps

Outline
• Simple Op Amps
  Two-stage
  Folded-cascode
• Summary
**SIMPLE TWO-STAGE OP AMPS**

**Two-Stage CMOS Op Amp Circuit:**

DC Conditions:
- $I_5 = I_{bias}$, $I_1 = I_2 = 0.5I_5 = 0.5I_{bias}$,
- $I_7 = I_6 = nI_{Bias}$

$V_{icm}(\text{max}) = V_{DD} - V_{SG3} + V_{T1}$

$V_{icm}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1}$

$V_{out}(\text{max}) = V_{DD} - V_{SD6}(\text{sat})$

$V_{out}(\text{min}) = V_{SS} + V_{DS7}(\text{sat})$

Notice that the output stage is class A

∴ $I_{sink} = I_7$ and $I_{source} = \frac{K_N'W_6}{2L_6} (V_{DD} - V_{SS} - V_T)^2 - I_7$
DC Balance Conditions for the Two-Stage Op Amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages. Therefore, we develop conditions to force M4 to be in saturation.

1.) First assume that $V_{SG4} = V_{SG6}$. This will cause “proper mirroring” in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is “guaranteed” to be in saturation.

2.) Let $S_i = \frac{W_i}{L_i}$, if $V_{SG4} = V_{SG6}$, then $I_6 = \left(\frac{S_6}{S_4}\right)I_4$.

3.) However, $I_7 = \left(\frac{S_7}{S_5}\right)I_5 = \left(\frac{S_7}{S_5}\right)(2I_4)$.

4.) For balance, $I_6$ must equal $I_7 \Rightarrow \frac{S_6}{S_4} = \frac{2S_7}{S_5}$ which is called the “balance conditions”.

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.
Small-Signal Performance of the Two-Stage CMOS Op Amp

Fig. 440-03
Small-Signal Performance of the Two-Stage CMOS Op Amp

Summary of the small signal performance:

Midband performance-

\[ A_0 = g_m I g_m II R_1 R_II \approx g_m 1 g_m 6 (r_{ds2} || r_{ds4})(r_{ds6} || r_{ds7}) , \quad R_{out} = r_{ds6} || r_{ds7} , \quad R_{in} = \infty \]

Roots-

Zero = \( \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c} \)

Poles at \( p_1 \approx \frac{-1}{g_{mII} R_1 R_{II} C_c} = \frac{- (g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6} C_c} \) and \( p_2 \approx \frac{-g_{mII}}{C_{II}} \approx \frac{-g_{m6}}{C_{L}} \)

Assume that \( g_m 1 = 100\mu S , \quad g_{m6} = 1mS , \quad r_{ds2} = r_{ds4} = 2M\Omega \quad r_{ds6} = r_{ds7} = 0.5M\Omega \), \( C_c = 5pF \) and \( C_{L} = 10pF \):

\[ A_0 = (100\mu S)(1M\Omega)(1000\mu S)(0.25M\Omega) = 25,000V/V \quad R_{in} = \infty \quad R_{out} = 250k\Omega \]

Zero = \( 1000\mu S/5pF = 2x10^8 \text{ rads/sec or } 31.83\text{MHz} \),

\[ p_1 = \frac{-1}{(1mS)(1M\Omega)(0.25M\Omega)(5pF)} = -800 \text{ rads/sec or } 127.3\text{Hz} , \quad GB = 3.178\text{MHz} \]

and \( p_2 = (-1000\mu S/10pF) = 10^8 \text{ rads/sec or } 15.915\text{MHz} \)
Slew Rate of a Two-Stage CMOS Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

\[ I_{\text{lim}} = C \frac{dv_C}{dt} \]

where \( v_C \) is the voltage across the capacitor \( C \).

\[ \text{Positive Slew Rate} \]

\[ SR^+ = \min \left[ \frac{I_5}{C_c}, \frac{I_6-I_5-I_7}{C_L} \right] = \frac{I_5}{C_c} \text{ because } I_6 \gg I_5 \]

\[ \text{Negative Slew Rate} \]

\[ SR^- = \min \left[ \frac{I_5}{C_c}, \frac{I_7-I_5}{C_L} \right] = \frac{I_5}{C_c} \text{ if } I_7 \gg I_5. \]

Therefore, if \( C_L \) is not too large and if \( I_7 \) is significantly greater than \( I_5 \), then the slew rate of the two-stage op amp should be,

\[ SR = \frac{I_5}{C_c} \]
Folded Cascode, CMOS Op Amp

Circuit:

Comments:

- The bias currents, $I_4$ and $I_5$, should be designed so that $I_6$ and $I_7$ never become zero (i.e. $I_5 = I_6 = 1.5I_3$)
- This amplifier is nearly balanced (would be exactly if $R_A$ was equal to $R_B$)
- Self compensating
- Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if $R_A$ and $R_B$ are greater than $g_{m1}$ or $g_{m2}$.)
Small-Signal Analysis of the Folded Cascode Op Amp

Model:
Recalling what we learned about the resistance looking into the source of the cascode transistor;

\[ R_A = \frac{r_{ds6} + R_2 + (1/gm10)}{1 + gm6r_{gs6}} \approx \frac{1}{gm6} \] and \[ R_B = \frac{r_{ds7} + R_{II}}{1 + gm7r_{ds7}} \approx \frac{R_{II}}{gm7r_{ds7}} \] where \( R_{II} \approx gm9r_{ds9}r_{ds11} \)

The small-signal voltage transfer function can be found as follows. The current \( i_{10} \) is written as

\[ i_{10} = \frac{-gm1(r_{ds1}||r_{ds4})v_{in}}{2[R_A + (r_{ds1}||r_{ds4})]} \approx \frac{-gm1v_{in}}{2} \]

and the current \( i_7 \) can be expressed as

\[ i_7 = \frac{gm2(r_{ds2}||r_{ds5})v_{in}}{2\left[\frac{R_{II}}{gm7r_{ds7}} + (r_{ds2}||r_{ds5})\right]} = \frac{gm2v_{in}}{2(1+k)} \] where \( k = \frac{R_{II}(g_{ds2}+g_{ds4})}{gm7r_{ds7}} \)

The output voltage, \( v_{out} \), is equal to the sum of \( i_7 \) and \( i_{10} \) flowing through \( R_{out} \). Thus,

\[ \frac{v_{out}}{v_{in}} = \left(\frac{gm1}{2} + \frac{gm2}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)gmIR_{out} \]
Frequency Response of the Folded Cascode Op Amp

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

\[ p_{out} = -\frac{1}{R_{out}C_{out}} \]

where \( C_{out} \) is all the capacitance connected from the output of the op amp to ground. All other poles must be greater than \( GB = \frac{g_{m1}}{C_{out}} \). The approximate expressions for each pole is

1.) Pole at node A: \( p_A \approx -\frac{1}{R_A C_A} \)

2.) Pole at node B: \( p_B \approx -\frac{1}{R_B C_B} \)

3.) Pole at drain of M6: \( p_6 \approx \frac{-1}{(R_2+1/g_{m10})C_6} \)

4.) Pole at source of M8: \( p_8 \approx -\frac{g_{m8}}{C_8} \)

5.) Pole at source of M9: \( p_9 \approx -\frac{g_{m9}}{C_9} \)

6.) Pole at gate of M10: \( p_{10} \approx -\frac{g_{m10}}{C_{10}} \)

where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because \( R_B \) is approximately \( r_{ds} \) that this pole might be too small. However, at frequencies where this pole has influence, \( C_{out} \), causes \( R_{out} \) to be much smaller making \( p_B \) also non-dominant.
Example 1 - Folded Cascode, CMOS Op Amp

Assume that all $g_{mN} = g_{mP} = 100\mu S$, $r_{dsN} = 2\Omega$, $r_{dsP} = 1\Omega$, and $C_L = 10pF$. Find all of the small-signal performance values for the folded-cascode op amp.

$$R_{II} = 0.4G\Omega, R_A = 10k\Omega, \text{ and } R_B = 4M\Omega : \ k = \frac{0.4 \times 10^9 (0.3 \times 10^{-6})}{100} = 1.2$$

$$v_{out} \over v_{in} = \left( \begin{array}{c} \frac{2}{2} + 1.2 \\ \frac{2}{2} + 2.2 \end{array} \right) (100)(57.143) = 4,354V/V$$

$$R_{out} = R_{II} \left[ \frac{g_{m7}r_{ds7}(r_{ds5})r_{ds2}}{g_{m7}r_{ds7}(r_{ds5})r_{ds2}} \right] = 400M\Omega \left[ (100)(0.667M\Omega) \right] = 57.143M\Omega$$

$$|P_{out}| = \frac{1}{R_{out}C_{out}} = \frac{1}{57.143M\Omega \cdot 10pF} = 1,750 \text{ rads/sec.} \Rightarrow 278Hz \Rightarrow GB = 1.21MHz$$

Comments on the Folded Cascode, CMOS Op Amp:

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required
SUMMARY

- Two stage op amp gives reasonably robust performance as an “on-chip” op amp
- DC balance conditions insure proper mirroring and all transistors in saturation
- Slew rate of the two-stage op amp is $I_5/C_c$
- Folded cascode op amp offers wider input common voltage range
- Folded cascode op amp is a self-compensated op amp because of the dominant pole at the output