ECE 4430
Project 2: Design of Operational Amplifier
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I have neither given nor received any unauthorized assistance on this project.
Design Summary

- **Design Environment**: Cadence Virtuosos, LTSpice, ADS
- **Technology**: Baker’s 50nm CMOS process
- **Supply**: 1 V
- **Topology**: Folded cascode differential amplifier + push-pull output stage
Schematic of Op-Amp

Note: DC current under loaded, zero AC input condition with common-mode voltage of 500 mV.

\[ I_1 = 15.3 \, \text{uA} \]
\[ I_2 = 3.27 \, \text{uA} \]
\[ I_3 = 9.224 \, \text{uA} \]
\[ I_4 = 9.243 \, \text{uA} \]
\[ I_5 = 15.3 \, \text{uA} \]
\[ I_6 = 15.2 \, \text{uA} \]
\[ I_{out} = 60.31 \, \text{uA} \]

PMOS Diff Pair

NMOS Diff Pair

Diff Pair Summing & Floating Current Source

Push Pull output

Design Process—Diff Pairs

• M5 and M14 represent the tail current source of the PMOS diff pair, and M15 and M10 represent the tail current source of the NMOS diff pair. To reduce the overdrive voltage of these transistors so as to increase ICMR, W/L’s of these four transistors were made large with the constraint that the tail current should avoid excessive power consumption.

• M2, M3, M4, and M9 represent the input transistors of the two diff pairs. Therefore, to obtain large CMRR, the W/L’s of these four transistors were maximized to reduce $v_{gs}$ for a given $v_{in}$. In addition, the tail current is sized to keep these four transistors in saturation.

• Length of M5, M14, and M15 (tail current source transistors) increased beyond 2*minimum feature size to mitigate channel-length modulation and increase output resistance with constraints of keeping tail current high and occupying small chip area.

• While diff gain is mostly determined by the diff pair, the common mode gain is found to be affected by every transistor in the summing circuit.
Design Process—Summing Circuit

- Recognize that transistors M20, M21, M59, and M60 form a PMOS folded cascode current mirror and that transistors M22, M23, M63, and M62 form an NMOS folded cascode current mirror. Therefore, the dimensions of M20 and M59 should be equal, as should the dimensions of M21 and M60, M22 and M63, and M23 and M62.

- To form an effective current mirror, channel-length modulation needs to be as mitigated as possible, meaning that length of each transistor should be reasonably large. At the same time, length must be kept sufficiently small so as to keep a sufficiently high W/L to maintain appropriate voltage biasing.

- Recall that since length is inversely proportional to λ (channel-length modulation constant) and that since $r_o \propto \frac{1}{\lambda I_D}$, a larger length tends to make $r_o$ larger. A larger $r_o$ enables small-signal changes in one branch of the summing circuit to be mirrored more accurately.

- Because the slew rate is affected mainly by the output buffer and floating current source, the main cascode branch is sized to conduct minimal current, which reduces the power consumption.
Chose push-pull topology with output transistors (M70 and M71) as well as floating current source transistors (M66-M69) because:
  - $R_{\text{load}}$ is large, so its effect on gain degradation is minimal.
  - The topology has high power efficiency.
  - The topology is capable of wide output swing.

From slew rate (SR) and loading specifications, output current should be:
$$I_{\text{OUT, MINIMUM}} = \text{SR} \times C_{\text{load}} = (40 \times 10^6 \text{ V/s}) \times (10^{-12} \text{ F}) = 40 \mu\text{A}$$

The W/L ratios of transistors M66-M69 were tuned such that their $V_{\text{DS}}$ values, i.e., the floating battery voltages, biased the output stage on the verge of turning on. This reduces the quiescent power consumption while still satisfying the slew rate requirement.

The floating current source transistors are placed on both sides of the main cascode summing circuit to minimize input referred offset voltage.

Capacitive compensation (C0 and C7) are employed to provide phase margin. Two compensation caps are found to provide better large signal response than one cap.
Beta multiplier reference from Project 1 is used due to its tunability and low power. The reference voltage was generated by tuning the resistor load.

In a realistic design project, the reference voltage will be generated by a master-slave current mirror, and therefore is less sensitive to process variation and occupies much less chip area.
Simulation Test Benches

**Step response:** use pulse mode in `vsource` from Cadence analogLib as input step voltage; perform transient analysis to see $v_{out}$

**ICMR:** use `vdc` from analogLib as input; perform DC sweep of $V_{in}$ from 0-1V and monitor $V_{out}$ voltage

**Gain($f_T$):** use `vsin` from analogLib as input with AC magnitude=1 and DC of 0.5V; perform AC analysis and monitor $V_{out}$ frequency response

**AC transient:** use `vsin` from analogLib with DC=0.5V and amplitude of 0.5V; perform transient simulation and measure output spectrum and THD

**Noise:** use `vdc` of 0.5V at the input; perform noise analysis for output voltage. Then plot equivalent input noise

**Output swing:** use 200k and 2M resistor in non-inverting amplifier topology; perform DC sweep of $V_{in}$ from 0-1V, monitor $V_{out}$ voltage

**Common mode gain (bottom setup):** sweep input small signal and monitor output response

**CMRR:** perform AC analysis of $v_{in}$; monitor $v_{out,d}/v_{out,c}$
Simulation Test Benches

Open loop gain and differential gain: use $vdc$ with DC magnitude of 80mV and AC magnitude of 1; perform AC analysis of $Vout$.

Note: For unloaded diff gain, the setup is identical to the top setup in CMRR, i.e. without the load in the above figure.

PSRR: use two $vdc$ sources, one as VDD and one as GND. The VDD source should have DC of 1. Then, set VDD (but not GND) to AC magnitude 1 and perform AC analysis at $Vout$ for PSRR+; set GND (but not VDD) to AC magnitude of 1 and perform AC analysis at $Vout$ for PSRR-.
Differential Gain and Phase

- **Phase margin** = $180^\circ - 132.1^\circ = 47.9^\circ$
- **Bandwidth** = 7.9 kHz
- **Differential Gain** = 84.5 dB
CMRR and Common-Mode Gain

- $\text{Acm (common mode gain)} = -62.3 \text{ dB}$
- $\text{CMRR} = 146.86 \text{ dB}$
The resistive divider of 200k and 2M in non-inverting amplifier creates an AC gain of 11, which is the expected ideal closed-loop gain of a non-inverting amplifier.
Low-to-High Step Response

- **Rise time** = time of 10% to 90% of the transition
  
  \[= 31.58 \text{ ns} - 21.22 \text{ ns} = 10.36 \text{ ns}\]

- **Slew rate** = \(\Delta V / \text{Rise time} = (0.82V - 0.18V) / 10.36 \text{ ns} = 61 \text{ V/µs}\)

- **Settling time** = time for output to come within 1% of the transition amount
  
  \[= 58 \text{ ns} - 20 \text{ ns} = 38 \text{ ns}\]
High-to-Low Step Response

- **Fall time** = time from 90% to 10% of the transition
  \[= 125.3\text{ ns} - 121\text{ ns} = 4.3\text{ ns}\]

- **Slew rate** = \(\Delta V/\text{Fall time} = (0.18\text{ V} - 0.82\text{ V}) / 4.3\text{ ns} = 148\text{ V/\mu s}\)

- **Settling time** = time for output to come within 1% of the transition amount
  \[= 132.87\text{ ns} - 120\text{ ns} = 12.87\text{ ns}\]
ICMR and Output Swing

- **ICMR** = 3.58mV ~ 992.45 mV
  ≃ 0 ~ 1V

- **Output swing** = 49.85 mV ~ 997.35 mV
  ≃ 50mV ~ 1V
Power Supply Rejection Ratio

- \( \text{PSRR}^+ = -54.13 \, \text{dB} \)
- \( \text{PSRR}^- = -8.622 \, \text{dB} \)
Noise

- Input referred noise $\leq 7.7 \mu V/\sqrt{Hz}$
Limitations and Improvements

- Differential gain can be made higher to meet the design specification with a gain enhancement op-amp, as in Baker’s book. However, brief exploration shows this technique could enhance common mode gain more than diff gain.

- A regulated drain current mirror can be used in diff pair tail current, such that the common mode gain will be further reduced, thereby enhancing the CMRR.

- The output voltage of the reference generator could be provided by the current mirror instead of resistor to offer accurate matching in layout and reduced process sensitivity.

- While all transistor dimensions are a multiple of the minimum feature size (50nm), the sizing of some transistors are sensitive to process variations. In a real tapeout, all transistors will be multiples of a base transistor size.

- The output stage can be cascoded to offer higher gain, though it could reduce the output voltage swing.

- Phase margin can be further improved using a larger compensation capacitor, but that could lead to further bandwidth reduction and slower transient response.
<table>
<thead>
<tr>
<th>Spec</th>
<th>Target</th>
<th>Achieved</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Supply Voltage (V)</td>
<td>N/A</td>
<td>0.56</td>
</tr>
<tr>
<td>Maximum Supply Voltage (V)</td>
<td>N/A</td>
<td>1.68</td>
</tr>
<tr>
<td>Gain of differential amplifier (dB) unloaded</td>
<td>&gt; 90</td>
<td>85.19</td>
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<tr>
<td>Gain of differential amplifier (dB) loaded</td>
<td>&gt; 110</td>
<td>146.9</td>
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<tr>
<td>CMRR (dB) (Low freq and spectrum)</td>
<td>&gt; 110</td>
<td>146.9</td>
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<tr>
<td>Reference power consumption (uW)</td>
<td>N/A</td>
<td>9</td>
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<tr>
<td>OpAmp power consumption with zero input (uW)</td>
<td>&lt; 150</td>
<td>92.4</td>
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<tr>
<td>OpAmp power consumption with no load (uW)</td>
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<td>90.17</td>
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<tr>
<td>Total power consumption (uW)</td>
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<td>101.4</td>
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<td>Positive Slew Rate (V/us)</td>
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<td>61</td>
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<tr>
<td>Negative Slew Rate (V/us)</td>
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</tr>
<tr>
<td>ICMR (Vmin ~ Vmax)</td>
<td>0 ~ 1</td>
<td>0 ~ 1</td>
</tr>
<tr>
<td>Output Swing (Vmin ~ Vmax)</td>
<td>0.1 ~ 0.9</td>
<td>0.05 ~ 1</td>
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<td>VDD PSRR (dB)</td>
<td>N/A</td>
<td>-54.13</td>
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<td>GND PSRR (dB)</td>
<td>N/A</td>
<td>-8.6</td>
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## Specification Summary

<table>
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<tr>
<th>Spec</th>
<th>Target</th>
<th>Achieved</th>
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<tbody>
<tr>
<td>Nominal output voltage (V)</td>
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<td>Input offset voltage (mV)</td>
<td>N/A</td>
<td>15.25</td>
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<td>Unloaded Bandwidth (kHz)</td>
<td>&gt; 10</td>
<td>7.32</td>
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<tr>
<td>Loaded Bandwidth (kHz)</td>
<td>&gt; 10</td>
<td>7.9</td>
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<td>Gain-bandwidth product (MHz)</td>
<td>N/A</td>
<td>169.7</td>
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<td>Compensation capacitor (pF)</td>
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<td>Phase margin (degrees)</td>
<td>&gt; 60</td>
<td>47.9</td>
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<tr>
<td>Rise time (ns) (Step response)</td>
<td>N/A</td>
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<tr>
<td>Fall time (ns) (Step response)</td>
<td>N/A</td>
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<tr>
<td>Settling time (ns) (Step response) (Low-to-High Transition)</td>
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<td>38</td>
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<tr>
<td>Settling time (ns) (Step response) (High-to-Low Transition)</td>
<td>N/A</td>
<td>12.87</td>
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<tr>
<td>Input referred noise (V/Hz^0.5)</td>
<td>N/A</td>
<td>7.7 x 10^-6</td>
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<td>THD for full swing output (%)</td>
<td>N/A</td>
<td>0.247</td>
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