Project #2: Design of an Operational Amplifier

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I have neither given nor received any unauthorized assistance on this project.

Process: Baker’s 50nm
CAD Tool: Cadence Virtuoso

Topology Selection: Input

- Input topology decided by ICMR (0.2–1V) for a supply voltage of 1.2V
- Use folded cascode topology for high input swing
- PMOS folded cascode (shown in figure):
  - $V_{in,min} = V_{OVN} - V_{THP} - V_{SS} = -210\text{mV}$
  - $V_{in,max} = V_{DD} - 2V_{OVP} - V_{THN} = 780\text{mV}$
- NMOS version would have the same limitation on the minimum input voltage

Solution: Use parallel NMOS and PMOS folded cascode differential pair for the input stage.
Topology Selection: Output

- Output topology decided by output swing (0.2–1V)
- Low output resistance is desirable
- Class AB Source follower buffer (shown in Figure)
  - $V_{\text{out, min}} = 2V_{\text{OV}} + V_{\text{THP}} - V_{\text{SS}} = 420\text{mV}$
  - $V_{\text{in, max}} = V_{\text{DD}} - 2V_{\text{OV}} - V_{\text{THN}} = 780\text{mV}$
- Must use class AB Push-Pull amplifier, which will also be a second gain stage

Selected Topology

- **Selected Topology:**
  - **Input:** Parallel NMOS and PMOS Folded Cascode
  - **Output/Second Stage:** Push-Pull Amplifier
- **Benefits**
  - Rail to Rail input
  - High Swing output
  - Higher Gain
- **Drawbacks**
  - Gain is not constant across input range (not an issue due to high open loop gain)
  - Gain highly dependent on resistive load
  - Added power consumption due to parallel differential amplifier
Design

• For SR of 120V/us
  – IT = SR*C_L = 120 uA
• Current in cascode branch is 1.2 – 1.5 times the tail current
• For parallel differential pairs (required to meet ICMR), we need more than, which is over the required power
• After literature review, no circuit was found (in research or industry) that meets all the criteria for this project.
• We decided to sacrifice SR and BW in order to save power
• Tail current chosen: 40 uA
• This means that our SR should be around 40 V/us

Design

• Because we are no longer concerned with ICMR, we can choose any overdrive voltage for the input differential pair.
• Let’s choose 50mV to obtain higher gm.

\[ gm_p = gm_n = \frac{2I_D}{V_{OV}} = 800 \mu S \]

• This would require W/L of NMOS input pairs to be around 150/2 = 7.5u/100n and PMOS to be 300/2 = 15u/100n
• Cascode transistors were chosen to conduct 1.3 times current in one side of the differential pair to prevent them from turning on.
Design

- Output stage is a push pull amplifier, sized to conduct 20uA
- Cascode device was added to increase output resistance and gain
- Compensation capacitor was added before the cascode device to use the cascode as a buffer
  - This helped greatly with the frequency response of the amplifier but did not remove the RHPZ
  - Resulted in bigger compensation capacitor because now the miller capacitance is in series with the CDS of the cascode device, reducing the effective capacitance
  - Zero nulling resistor was added to remove RHPZ

Reference Schematic

Used topology in Baker’s Figure 20.47

Resistor value changed to obtain desired currents
Amplifier Schematic

Complementary Folded Cascode Differential Pair

Push/Pull Output Stage

Simulation Test benches

Inductor in feedback
Open Loop Gain: Frequency sweep at input $A_{ol}$
Frequency sweep with shorted inputs

Buffer configuration
ICMR: DC sweep from 0.2 to 1.4
SR: Step from 0.1 to 1.1 V
THD: 1kHz Sine wave covering full output swing

Non-inverting Amplifier
Output Swing: Sweep input from 0.2 to 1.4 and see where output saturates

Note: Infini-leak inductor is used to act as a short in DC but open in AC. It allows for Cadence to calculate the DC operating point correctly.

Note: Infini-leak inductor is used as an open in DC, and the same simulation values were obtained.

Probe acts as a short in DC but open in AC. This is the same as using an infinite inductor.

Probe was used in Open Loop Gain because it was easier to simulate CMRR.

Note: Perform noise analysis on Cadence
Open Loop Response

Input and Output Swing
# Spec Summary

<table>
<thead>
<tr>
<th>Spec</th>
<th>Target</th>
<th>Achieved</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential amplifier topology</td>
<td>N/A</td>
<td>Parallel Folded Cascode</td>
</tr>
<tr>
<td>Reference topology</td>
<td>N/A</td>
<td>Baker 50 nm</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Loading (pF</td>
<td></td>
<td>kOhm)</td>
</tr>
<tr>
<td>Differential Gain (dB)</td>
<td>80</td>
<td>80.23</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>120</td>
<td>94.76</td>
</tr>
<tr>
<td>ICMR (V)</td>
<td>0.2 - 1</td>
<td>56m – 1.16</td>
</tr>
<tr>
<td>Output Swing (V)</td>
<td>0.1 - 1.1</td>
<td>59m – 1.08</td>
</tr>
<tr>
<td>Bandwidth - 3dB (kHz) (Loaded/Unloaded)</td>
<td>100</td>
<td>18.47 / 1.69</td>
</tr>
<tr>
<td>Gainbandwidth product (MHz)</td>
<td>N/A</td>
<td>76.4</td>
</tr>
<tr>
<td>Compensation capacitor (pF)</td>
<td>N/A</td>
<td>See schematic</td>
</tr>
<tr>
<td>Phase margin (degrees)</td>
<td>45</td>
<td>45.86</td>
</tr>
<tr>
<td>Gain of differential amplifier (dB)</td>
<td>N/A</td>
<td>47.7</td>
</tr>
<tr>
<td>Max Power consumption (uW) (Loaded/Unloaded) (Buffer Configuration)</td>
<td>200</td>
<td>178.4 / 173.5</td>
</tr>
<tr>
<td>Reference power consumption (uW)</td>
<td>N/A</td>
<td>93.4</td>
</tr>
<tr>
<td>OpAmp power consumption with zero input (uW) (Buffer Configuration)</td>
<td>N/A</td>
<td>178.4</td>
</tr>
<tr>
<td>Total power consumption (uW)</td>
<td>N/A</td>
<td>271.8</td>
</tr>
<tr>
<td>Slew Rate (V/us) (Positive/Negative)</td>
<td>120 / -120</td>
<td>40 / -34.7</td>
</tr>
</tbody>
</table>

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**Noise**

- **Input referred noise (uV/√Hz)**
  - **freq (kHz)**
  - **Input referred noise (uV/√Hz)**
  - **10^0**
  - **30.0**
  - **20.0**
  - **10.0**
  - **0.0**
  - **-10.0**
  - **-20.0**
  - **-30.0**
- **freq (kHz)**
- **Input referred noise (uV/√Hz)**
- **10^0**
- **30.0**
- **20.0**
- **10.0**
- **0.0**
- **-10.0**
- **-20.0**
- **-30.0**

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**MG6**
Spec Summary Cont’d

<table>
<thead>
<tr>
<th>Spec</th>
<th>Target</th>
<th>Achieved</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V) (Maximum/Minimum)</td>
<td>N/A</td>
<td>0.55 / 3.00</td>
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<tr>
<td>Nominal output voltage (V)</td>
<td>N/A</td>
<td>0.6</td>
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<tr>
<td>Input offset voltage (mV)</td>
<td>N/A</td>
<td>-12</td>
</tr>
<tr>
<td>Rise/Fall time (ns) (to 90% of final value)</td>
<td>N/A</td>
<td>20 / 23</td>
</tr>
<tr>
<td>Settling time (ns) (Rising / Falling Edge)</td>
<td>N/A</td>
<td>160 / 109</td>
</tr>
<tr>
<td>RMS Input referred noise (V) (1 Hz – 100MHz) (Simulated in open loop)</td>
<td>N/A</td>
<td>7.51 n</td>
</tr>
<tr>
<td>THD for full swing output (%) (Simulated in Buffer mode)</td>
<td>N/A</td>
<td>1.165 %</td>
</tr>
</tbody>
</table>

How to improve design?

- To improve CMRR, make tail current sources longer to increase $R_{Tail}$

\[ A_{CM} = \frac{g_{mR_{OUT}}}{1 + g_{mR_{Tail}}} \]

- To improve SR, increase tail current and current at output stage.
- Ideally a buffer should be used for the output, but implementation of high-swing low impedance buffer is difficult. Using a buffer would make gain and bandwidth independent of loading
- Use advanced compensation techniques, such as those shown in the references, to reduce capacitor size and increase phase margin
- Better match currents in PMOS and NMOS differential pairs to reduce offset voltage. This can be done by selecting a different overdrive voltage for the input devices so that the tail current sources have a $V_{DS}$ that results in better current matching. Constant $g_{m}$ amplifier might also reduce this offset.
Conclusion

- Completed design of two stage operational amplifier
- Opted for low power operation instead of high speed (SR and Bandwidth)
- Parallel input differential pairs were necessary to meet ICMR requirements
- Push pull amplifier was needed to meet output swing requirements. Cascode devices were added to increase the gain and output resistance. However, buffer should be used for the output
- Design could be improved with relaxed power specifications

References