Georgia Institute of Technology
Department of Electrical and Computer Engineering

Exam 1

ECE-4430 Fall 2007
Monday, September 17, 2007 Duration: 50min

First name Solutions Last name Solutions

ID number __________________________

This is a close-book, close-note exam. You can use a standard engineering calculator (if needed). You can have a 2-sided sheet of equations and notes.

Show your work for partial credits. Remember to write your name on each page.

Please consider the following honor pledge. "I have neither given nor received any unauthorized assistance on this exam."

Signature __________________________

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Problem #1: Basic Device questions

For the following problem, assume we have the following pFET device with the voltage sources and output current as shown. You can assume that these devices have no back-gate effects, $V_{dd} = 3V$, and the threshold voltage is $-1V$. Identify all important regions and breakpoints in your plots.

a.) Plot below the relationship, both in linear and log-scale, between $I$ and $V_g$, assuming $V_d = 0$.

b.) Plot below the relationship between $I$ and $V_d$ for three different gate voltages. In one plot assume all three currents are in subthreshold, and in the other plot assume all three currents are in above threshold.

$V_{G1-3} = 2.7, 2.5, 2.3$  \[4V_T \approx 0.1V \]

$V_{G1-3} = 1.9, 1.5, 1V$
Problem #2: MOSFET Small Signal Modeling

This problem assumes a MOSFET circuit to the right, with the following parameters: \( I_{th} = 125 \text{nA}, \) \( K = 80 \text{ uA/V}^2, \) \( V_T = 0.6 \text{V}, \) \( V_A = 25 \text{V}. \) The drain voltage is biased at 2.5\text{V}; assume the MOSFET is in saturation throughout this problem. Also assume that \( k = 1. \)

(a) What is the minimum drain voltage bias required to keep this MOSFET in saturation as a function of gate voltage? This should be for both subthreshold and above-threshold operation.

\[
\text{Sub. Th. } V_d > 100 \text{ mV} = 4V_T \\
\text{Above Th. } V_d > V_g - V_T - V_T = V_g - 0.6 \text{V}
\]

(b) Compute and draw the small signal model of this MOSFET circuit (not including the capacitors yet). Evaluate the transconductance at a bias current of 100\text{nA} and 10\text{uA}.

\[
I_d = 100 \text{nA} < I_{th} \rightarrow \text{Sub. } \overline{V}_T \rightarrow \begin{align*}
\overline{g}_m &= \frac{I_d}{V_T} \\
&= \frac{100 \text{nA}}{0.6 \text{V}} \\
&= 4 \text{\mu S}
\end{align*}
\]

(c) Qualitatively, how would this model change for a BJT device instead of a MOSFET transistor (assume the collector replaces the drain and the base replaces the gate).

(d) Solve for the expression for the maximum gain from this device? Evaluate again at bias currents of 100\text{nA} and 10\text{uA}.

\[
\begin{align*}
\text{Max Gain} &= \overline{g}_m V_0 \\
\overline{V}_0 &= \frac{V_A}{I_d} \\
I_d = 100 \text{nA} \rightarrow V_0 &= \frac{25 \text{V}}{100 \text{nA}} = 250 \text{M\Omega} \\
&\rightarrow A_v(\text{max}) = 4 \times 10^{-6} \times 2.5 \times 10^8 \\
&= 1000 \\
I_d = 10 \text{\mu A} \rightarrow V_0 &= \frac{25 \text{V}}{10 \text{\mu A}} = 2.5 \text{M\Omega} \\
&\rightarrow A_v(\text{max}) = 40 \times 10^{-6} \times 2.5 \times 10^6 \\
&= 100
\end{align*}
\]
Problem #3: Circuit Analysis

(a) Indicate the type of amplifier shown in the following circuit.

(b) Find transistor drain currents with respect to $V_{dd}$, $R$, $V_{TN}$, and $V_{TP}$ (Ignore body effect and channel length modulation).

(c) Draw the small signal equivalent of this circuit and simplify it as much as possible.

(d) Using the small signal model, find the gain ($V_{out}/V_{in}$) of this amplifier parametrically (ignore body effect but consider channel length modulation).

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a) This circuit consists of a simple current mirror (i.e., current source) and a "Common Gate" amplifier.

b) Assuming $(W/L)_3 = (W/L)_2 \Rightarrow I_{D_1} = I_{D_2} = I_{D_3} = I_R$

KVL: $V_{SG_3} = V_{SG_2} = V_{DD} - R I_R$

Saturation: $I_{D_3} = \frac{K_3}{2} (V_{SG_3} - V_{TP})^2 = I_R$

$\Rightarrow I_R = \frac{K_3}{2} (V_{DD} - R I_R - V_{TP})^2 \rightarrow$ Solving this eq. will give bias current for all MOSFET based on other process dependent parameters and $V_{DD}$ & $R$.

Cont. Next Page.
c) The current mirror looking into the drain of M2 is just V_{o2}.

Now we can add this as a load to CB amplifier. V_{G1} is a DC voltage \Rightarrow Ground in AC small signal.

d) Writing KCL at output node:

\[ g_m V_{in} = \frac{V_{out} - V_{in}}{V_{o1}} = V_{out} \left( \frac{1}{V_{o1}} + \frac{1}{V_{o2}} \right) \]

\[ \Rightarrow \frac{V_{out}}{V_{in}} = \left( g_m + \frac{1}{V_{o1}} \right) \left( \frac{1}{V_{o1}} + \frac{1}{V_{o2}} \right) \]

Simplified small signal model.