3.3 - TWO-TRANSISTOR AMPLIFIERS

INTRODUCTION

Objective
The objective of this presentation is:
1.) Show how two transistors are used to achieve amplifiers with improved performance
2.) Show the analysis of multiple transistor amplifiers using resistive loads
3.) Continue to build the amplifier concepts necessary to consider integrated circuit amplifiers

Outline
• BJT CC-CE, CC-CC amplifiers
• Darlington transistor amplifier
• BJT-MOS amplifiers
• Cascode amplifiers
• Summary
BJT TWO TRANSISTOR AMPLIFIERS

The Common Collector-Common Emitter Configuration

Circuit:

Small-signal performance:

\[ R_{in} = r_{\pi 1} + (1 + \beta_o 1)r_{\pi 2} \]

\[ R_{out} = r_{o 2} \]

\[ \frac{v_{out}}{v_{in}} = - \frac{g_{m 2}(r_{o 2}||R_L)(1 + \beta_o 1)r_{\pi 2}}{R_{in}} = - \frac{\beta_o 2(r_{o 2}||R_L)(1 + \beta_o 1)}{r_{\pi 1} + (1 + \beta_o 1)r_{\pi 2}} \rightarrow -g_{m 2}(r_{o 2}||R_L) \]

\[ \frac{i_{out}}{i_{in}} = \frac{g_{m 2}(1 + \beta_o 1)r_{\pi 2}}{R_{in}} = \frac{\beta_o 2(1 + \beta_o 1)}{r_{\pi 1} + (1 + \beta_o 1)r_{\pi 2}} \rightarrow \beta_o 2(1 + \beta_o 1) \]

Increased input resistance and current gain.
Example 1 - Calculation of Small-Signal Performance for the CC-CC Configuration

Find the small-signal input resistance, output resistance, voltage gain, and current gain for the composite transistor shown. Assume for both devices, that $\beta_o = 100$, $r_b = 0$, and $r_o = \infty$. Assume for Q2 that $I_C = 100\mu A$ and that $I_{bias} = 10\mu A$.

**Solution**

The small-signal model is shown. The values of the parameters are found as,

\[
r_{\pi 1} = \frac{\beta_{o1} V_t}{I_{C1}} = \frac{100\cdot 26mV}{11\mu A} = 236k\Omega,
\]

\[
r_{\pi 2} = \frac{\beta_{o2} V_t}{I_{C2}} = \frac{100\cdot 26mV}{100\mu A} = 26k\Omega,
\]

and \[ g_{m2} = \frac{I_C}{V_t} = \frac{100\mu A}{26mV} = 38.4mS \]

\[ \therefore R_{in} = 236k\Omega + (100)26k\Omega = 2.84M\Omega \]

\[ R_{out} = 10k\Omega \text{ (if } R_L \text{ is included)} \]

\[ \frac{v_{out}}{v_{in}} = -\frac{\beta_{o2}(r_o)||R_L)(1+\beta_{o1})}{R_{in}} = -\frac{100\cdot10k\Omega\cdot101}{2.84M\Omega} = -35.56V/V \]

\[ \frac{i_{out}}{i_{in}} = \beta_{o2}(1+\beta_{o1}) = 100\cdot101 = 10,100A/A \]
Common Collector-Common Collector

Circuit:

Small-signal performance ($I_{Bias} \ll I_{C2}$):

$$R_{in} = r_{\pi 1} + (1 + \beta_{o1})(r_{\pi 2} + (1 + \beta_{o2})(r_o||R_L)) \approx (1 + \beta_{o1})(1 + \beta_{o2})(r_o||R_L)$$

$$R_{out} = \frac{R_S + r_{\pi 1}}{1 + \beta_{o1}} + \frac{r_{\pi 2}}{1 + \beta_{o2}} = \frac{R_S + r_{\pi 1} + r_{\pi 2}(1 + \beta_{o1})}{(1 + \beta_{o1})(1 + \beta_{o2})} \approx \frac{1}{g_{m2}}$$

$$\frac{v_{out}}{v_{in}} \approx 1$$

$$\frac{i_{out}}{i_{in}} = (1 + \beta_{o2})(1 + \beta_{o1})$$

Very high input resistance and very low output resistance.
Darlington Configuration

Circuit:

The Darlington configuration can be CE, CB, or CC.

For common-emitter ($\beta_o >> 1$) with a collector resistance of $R_L$:

$$R_{in} = r_{\pi 1} + (1+\beta_{o1})r_{\pi 2}, \quad R_{out} \approx r_{o2}$$

$$\frac{v_{out}}{v_{in}} = -\frac{\beta_{o1}\beta_{o2}R_L}{r_{\pi 1} + \beta_{o1}r_{\pi 2}}$$

Replacing $r_{\pi 1}$ and $r_{\pi 2}$ by their large-signal equivalents ($r_{\pi} = \frac{\beta_oV_t}{I_C}$) gives,

$$\frac{v_{out}}{v_{in}} = -\frac{\beta_{o1}\beta_{o2}R_L}{\beta_{o1}\beta_{o2}V_t + \beta_{o1}\beta_{o2}V_t} = -\frac{g_{m2}R_L}{2}$$

(Input “base-emitter” voltage is divided across the two transistors)
BiCMOS Darlington Configuration

Circuit:

For the common-emitter configuration \((\beta_o \gg 1 \text{ and } r_{ds1} \text{ negligible})\) with \(R_L >> r_{o2}\):

\[ R_{in} = \infty \]
\[ R_{out} \approx r_{o2} \]

\[ \frac{v_{out}}{v_{in}} = \left( \frac{v_{out}}{v_{gs1}} \right) \frac{v_{gs1}}{v_{in}} = \left( \frac{-g_{m1} + g_{m1}g_{m2}r_{\pi2}}{g_{o2}} \right) \left( \frac{1}{1 + g_{m1}r_{\pi2}} \right) = -\frac{g_{m1}(1 + g_{m2}r_{\pi2})}{g_{o2}(1 + g_{m1}r_{\pi2})} \approx -g_{m1}r_{o2} \text{ if } g_{m1} \approx g_{m2} \]

\[ \frac{i_{out}}{i_{in}} = \infty \]

Note that the input dc voltage consists of \(V_{GS} + V_{BE}\) which is around 2V.
CASCODE CONFIGURATION

**BJT Cascode Amplifier**

Circuit and small-signal model:

If $\beta_1 \approx \beta_2$ and $r_o$ can be neglected, then:

- $R_{in} = r_{\pi 1}$
- $R_{out} = \beta_2 r_{o2}$

\[
\frac{v_{out}}{v_{in}} = \left( \frac{v_{out}}{v_a} \right) \left( \frac{v_a}{v_{in}} \right) = (g_{m2}R_L) \left( \frac{r_{\pi 2}}{1 + \frac{r_{\pi 2}}{r_{\pi 1}}} \right) \approx (g_{m2}R_L) (-1) = -g_{m2}R_L
\]

\[
\frac{i_{out}}{i_{in}} = \alpha_2 \beta_1
\]

The advantage of the cascode is that the gain of Q1 is -1 and therefore the Miller capacitor, $C_\mu$, is not translated to the base-emitter as a large capacitor.
**BJT Cascode Amplifier Frequency Response**

Small-Signal Model with the Miller effect applied to $C_\mu_1$ assuming $v_a/v_{in} = -1$:

Find the -3dB frequency, $f_{-3dB}$ using the following formula:

$$f_{-3dB} \approx \frac{1}{2\pi \sum \text{(Open-circuit time constants)}}$$

$$\tau_{in} = r\pi_1(C\pi_1 + 2C_\mu_1), \quad \tau_{interstage} = \frac{r\pi_2}{1 + \beta_{o2}}(C\pi_2 + 2C_\mu_1), \quad \text{and} \quad \tau_{out} = R_L C_\mu_2$$

$$\therefore \quad f_{-3dB} \approx \frac{1}{2\pi \left( r\pi_1(C\pi_1 + 2C_\mu_1) + \frac{r\pi_2}{1 + \beta_{o2}}(C\pi_2 + 2C_\mu_1) + R_L C_\mu_2 \right)} \approx \frac{1}{2\pi R_L C_\mu_2}$$
MOS Cascode Amplifier

Circuit and small-signal model:

Small-signal performance (assuming a load resistance in the drain of $R_L$):

$$R_{in} = \infty$$

Using nodal analysis, we can write,

$$[g_{ds1} + g_{ds2} + g_m2]v_1 - g_{ds2}v_{out} = -g_{m1}v_{in}$$

$$-[g_{ds2} + g_m2]v_1 + (g_{ds2} + G_L)v_{out} = 0$$

Solving for $v_{out}/v_{in}$ yields,

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}(g_{ds2} + g_m2)}{g_{ds1}g_{ds2} + g_{ds1}G_L + g_{ds2}G_L + G_Lg_{m2}} = -\frac{g_{m1}}{G_L} = -g_{m1}R_L$$

Note that unlike the BJT cascode, the voltage gain, $v_1/v_{in}$ is greater than -1.

$$\frac{v_1}{v_{in}} = -g_m2\left[\frac{r_{ds2}}{1 + g_m2r_{ds2}}\right] \approx \frac{r_{ds2} + R_L}{r_{ds2}} = -\left(1 + \frac{R_L}{r_{ds2}}\right) \quad (R_L \text{ must be less than } r_{ds2} \text{ for the gain to be } -1)$$

The small-signal output resistance is,

$$r_{out} = [r_{ds1} + r_{ds2} + g_m2r_{ds1}r_{ds2}]||R_L \equiv R_L$$
MOS Cascode Amplifier Frequency Response

Small-signal model ($g_{m2}v_1$ has been rearranged and the substitution theorem applied):

\[ \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{1}{1 + as + b s^2} \left( \frac{-(g_{m1} - sC_1)(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + (g_{ds2} + G_L)(g_{m2} + g_{ds1} + g_{ds2})} \right) \]

where

\[ a = \frac{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3} + G_L) + C_1(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + (g_{ds3} + G_L)(g_{m2} + g_{ds1} + g_{ds2})} \]

and

\[ b = \frac{C_3(C_1 + C_2)}{g_{ds1}g_{ds2} + (g_{ds3} + G_L)(g_{m2} + g_{ds1} + g_{ds2})} \]

The nodal equations now become:

\[ (g_{m2} + g_{ds1} + g_{ds2} + sC_1 + sC_2)v_1 - g_{ds2}v_{\text{out}} = -(g_{m1} - sC_1)v_{\text{in}} \]

and

\[ -(g_{ds2} + g_{m2})v_1 + (g_{ds2} + g_{ds3} + G_L + sC_3)v_{\text{out}} = 0 \]

Solving for $V_{\text{out}}(s)/V_{\text{in}}(s)$ gives,

\[ \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{1}{1 + as + b s^2} \left( \frac{-(g_{m1} - sC_1)(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + (g_{ds2} + G_L)(g_{m2} + g_{ds1} + g_{ds2})} \right) \]
A Simplified Method of Finding an Algebraic Expression for the Two Poles

Assume that a general second-order polynomial can be written as:

\[ P(s) = 1 + as + bs^2 = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2} \]

Now if \(|p_2| >> |p_1|\), then \(P(s)\) can be simplified as

\[ P(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2} \]

Therefore we may write \(p_1\) and \(p_2\) in terms of \(a\) and \(b\) as

\[ p_1 = \frac{-1}{a} \quad \text{and} \quad p_2 = \frac{-a}{b} \]

Applying this to the previous problem gives,

\[ p_1 = \frac{-[g_{ds1}g_{ds2} + (g_{ds3}+G_L)(g_{m2} + g_{ds1} + g_{ds2})]}{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}+G_L) + C_1(g_{ds2} + g_{ds3}+G_L)} \approx \frac{-(g_{ds3}+G_L)}{C_3} \]

The nondominant root \(p_2\) is given as

\[ p_2 = \frac{-[C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}+G_L) + C_1(g_{ds2} + g_{ds3}+G_L)]}{C_3(C_1 + C_2)} \approx \frac{-g_{m2}}{C_1 + C_2} \]

Assuming that \(C_1\), \(C_2\), and \(C_3\) are the same order of magnitude, and that \(g_{m2}\) is greater than \(g_{ds3}\), then \(|p_1|\) is smaller than \(|p_2|\) (closer to the origin). Therefore the approximation of \(|p_2| >> |p_1|\) is valid.

Note that there is a right-half plane zero at \(z_1 = \frac{g_{m1}}{C_1}\).
**BiCMOS Cascode Amplifier**

Circuits:

![BiCMOS Cascode Amplifier Circuits](image)

Comparison:

<table>
<thead>
<tr>
<th>Q1</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Larger voltage gain</td>
<td>Infinite input resistance</td>
</tr>
<tr>
<td>Smaller input resistance</td>
<td>Smaller voltage gain</td>
</tr>
<tr>
<td>Q1 voltage gain greater than -1V/V</td>
<td>M1 voltage gain less than -1V/V</td>
</tr>
<tr>
<td>High output resistance</td>
<td>High output resistance</td>
</tr>
<tr>
<td>Requires input current</td>
<td>Does not require input current</td>
</tr>
</tbody>
</table>

2TA08
SUMMARY

Advantages of two-transistors:
- Higher input resistance (BJTs)
- Lower output resistance
- Higher current gain (BJTs)

Things that are important for future use:
- The upper -3dB frequency can be approximated by the reciprocal of the sum of the OTCs (p. 8)
- A quadratic can be solved algebraically by assuming the roots are widely spaced (p. 11)