6.2 INTRODUCTION TO OP AMPS

INTRODUCTION

Objective
The objective of this presentation is:
1.) Characterize the operational amplifier
2.) Illustrate the analysis of both BJT and MOS op amps
3.) Illustrate the design of both BJT and MOS op amps

Outline
• Introduction and Characterization of Op Amps
• Compensation of Op Amps
  General principles
  Miller, Nulling Miller
  Self-compensation
  Feedforward
• Simple Op Amps
  Two-stage
  Folded-cascode
• Design of Op Amps
• Summary
INTRODUCTION AND CHARACTERIZATION OF OP AMPS

High-Level Viewpoint of an Op Amp

Block diagram of a general, two-stage op amp:

- Differential transconductance stage:
  Forms the input and sometimes provides the differential-to-single ended conversion.
- High gain stage:
  Provides the voltage gain required by the op amp together with the input stage.
- Output buffer:
  Used if the op amp must drive a low resistance.
- Compensation:
  Necessary to keep the op amp stable when resistive negative feedback is applied.
**Ideal Op Amp**

Symbol:

![Ideal Op Amp Symbol](image)

Null port:
If the differential gain of the op amp is large enough then input terminal pair becomes a null port.
A null port is a pair of terminals where the voltage is zero and the current is zero.
I.e.,
\[ v_1 - v_2 = v_i = 0 \]
and
\[ i_1 = 0 \text{ and } i_2 = 0 \]
Therefore, ideal op amps can be analyzed by assuming the differential input voltage is zero and that no current flows into or out of the differential inputs.
General Configuration of the Op Amp as a Voltage Amplifier

Noninverting voltage amplifier:

\[ v_{inn} = 0 \implies v_{out} = \frac{R_1 + R_2}{R_1} v_{inp} \]

Inverting voltage amplifier:

\[ v_{inp} = 0 \implies v_{out} = \frac{R_2}{R_1} v_{inn} \]
Example 1 - Simplified Analysis of an Op Amp Circuit

The circuit shown below is an inverting voltage amplifier using an op amp. Find the voltage transfer function, \( v_{\text{out}}/v_{\text{in}} \).

![Virtual Ground Fig. 6.1-4](image)

Solution

If the differential voltage gain, \( A_v \), is large enough, then the negative feedback path through \( R_2 \) will cause the voltage \( v_i \) and the current \( i_i \) shown on Fig. 6.1-4 to both be zero. Note that the null port becomes the familiar virtual ground if one of the op amp input terminals is on ground. If this is the case, then we can write that

\[
i_1 = \frac{v_{\text{in}}}{R_1}
\]

and

\[
i_2 = \frac{v_{\text{out}}}{R_2}
\]

Since, \( i_i = 0 \), then \( i_1 + i_2 = 0 \) giving the desired result as

\[
\frac{v_{\text{out}}}{v_{\text{in}}} = - \frac{R_2}{R_1}.
\]
Linear and Static Characterization of the Op Amp

A model for a nonideal op amp that includes some of the linear, static nonidealities:

\[ v_2 \]
\[ v_1 \]
\[ \frac{v_1}{CMRR} \]
\[ R_{icm} \]
\[ I_{B2} \]
\[ e_n^2 \]
\[ I_{B1} \]
\[ C_{id} \]
\[ R_{id} \]
\[ R_{out} \]
\[ v_{out} \]

where

- \( R_{id} \) = differential input resistance
- \( C_{id} \) = differential input capacitance
- \( R_{icm} \) = common mode input resistance
- \( V_{OS} \) = input-offset voltage
- \( I_{B1} \) and \( I_{B2} \) = differential input-bias currents
- \( I_{OS} \) = input-offset current \( (I_{OS} = I_{B1} - I_{B2}) \)
- \( CMRR \) = common-mode rejection ratio
- \( e_n^2 \) = voltage-noise spectral density (mean-square volts/Hertz)
- \( i_n^2 \) = current-noise spectral density (mean-square amps/Hertz)
Linear and Dynamic Characteristics of the Op Amp

Differential and common-mode frequency response:

$$V_{out}(s) = A_v(s)[V_1(s) - V_2(s)] \pm A_c(s) \left( \frac{V_1(s) + V_2(s)}{2} \right)$$

Differential-frequency response:

$$A_v(s) = \frac{A_{v0}}{ \left( \frac{s}{p_1} - 1 \right) \left( \frac{s}{p_2} - 1 \right) \left( \frac{s}{p_3} - 1 \right) \cdots } = \frac{A_{v0} p_1 p_2 p_3 \cdots}{(s-p_1)(s-p_2)(s-p_3)\cdots}$$

where $p_1, p_2, p_3, \cdots$ are the poles of the differential-frequency response.

Fig. 6.1-6
Other Characteristics of the Op Amp

Power supply rejection ratio (PSRR):

\[ PSRR = \frac{\Delta V_{DD}}{\Delta V_{OUT}} \cdot A_v(s) = \frac{V_o/V_{in} (V_{dd} = 0)}{V_o/V_{dd} (V_{in} = 0)} \]

Input common mode range (ICMR):

\[ ICMR = \text{the voltage range over which the input common-mode signal can vary without influence the differential performance} \]

Slew rate (SR):

\[ SR = \text{output voltage rate limit of the op amp} \]

Settling time (T_s):

\[ T_s = \text{time needed for the output of the op amp to reach a final value to with a predetermined tolerance when excited by a small signal. (SR is large signal excitation)} \]
Classification of CMOS Op Amps

Categorization of op amps:

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</tr>
<tr>
<td></td>
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</tr>
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First Voltage Stage

Second Voltage Stage

Current Stage

Table 6.1-1
**Two-Stage Op Amp Architecture**

Simple two-stage op amp broken into voltage-to-current and current-to-voltage stages:
**Folded-Cascode Op Amp Architecture**

Simple folded-cascode op amp broken into voltage-to-current and current-to-voltage stages:
COMPENSATION OF OP AMPS

GENERAL PRINCIPLES

Objective

Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
   - Miller capacitor only
   - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
   - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.

2. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

3. Self compensating - Load capacitor compensates the op amp.
Single-Loop, Negative Feedback Systems

\[ A(s) = \text{amplifier gain (normally the differential-mode voltage gain of the op amp)} \]
\[ F(s) = \text{transfer function of the external feedback from the output of the op amp back to the input.} \]

Definitions:
- Open-loop gain = \( L(s) = -A(s)F(s) \)
- Closed-loop gain = \( \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{A(s)}{1+A(s)F(s)} \)

Stability Requirements:
The requirements for stability for a single-loop, negative feedback system is,
\[ |A(j\omega_0)F(j\omega_0)| = |L(j\omega_0)| < 1 \]
where \( \omega_0 \) is defined as
\[ \text{Arg}[-A(j\omega_0)F(j\omega_0)] = \text{Arg}[L(j\omega_0)] = 0^\circ \]

Another convenient way to express this requirement is
\[ \text{Arg}[-A(j\omega_{0\text{dB}})F(j\omega_{0\text{dB}})] = \text{Arg}[L(j\omega_{0\text{dB}})] > 0^\circ \]
where \( \omega_{0\text{dB}} \) is defined as
\[ |A(j\omega_{0\text{dB}})F(j\omega_{0\text{dB}})| = |L(j\omega_{0\text{dB}})| = 1 \]
Illustration of the Stability Requirement using Bode Plots

A measure of stability is given by the phase when \(|A(j\omega)F(j\omega)| = 1\). This phase is called \(\text{phase margin}\).

Phase margin = \(\Phi_M = \text{Arg}\{-A(j\omega_{0\text{dB}})F(j\omega_{0\text{dB}})\} = \text{Arg}\{L(j\omega_{0\text{dB}})\}\)
Why Do We Want Good Stability?

Consider the step response of second-order system which closely models the closed-loop gain of the op amp.

A “good” step response is one that quickly reaches its final value. Therefore, we see that phase margin should be at least 45° and preferably 60° or larger. (A good rule of thumb for satisfactory stability is that there should be less than three rings.)
Uncompensated Frequency Response of Two-Stage Op Amps

Two-Stage Op Amps:

Small-Signal Model:

Note that this model neglects the base-collector and gate-drain capacitances for purposes of simplification.
Uncompensated Frequency Response of Two-Stage Op Amps - Continued

For the MOS two-stage op amp:

\[ R_1 \approx \frac{1}{g_{m3}} || r_{ds3} || r_{ds1} \approx \frac{1}{g_{m3}} \]
\[ R_2 = r_{ds2} || r_{ds4} \quad \text{and} \quad R_3 = r_{ds6} || r_{ds7} \]
\[ C_1 = C_{gs3} + C_{gs4} + C_{bd1} + C_{bd3} \quad C_2 = C_{gs6} + C_{bd2} + C_{bd4} \quad \text{and} \quad C_3 = C_L + C_{bd6} + C_{bd7} \]

For the BJT two-stage op amp:

\[ R_1 = \frac{1}{g_{m3}} || r_{\pi3} || r_{\pi4} || r_{o3} \approx \frac{1}{g_{m3}} \]
\[ R_2 = r_{\pi6} || r_{o2} || r_{o4} \approx r_{\pi6} \quad \text{and} \quad R_3 = r_{o6} || r_{o7} \]
\[ C_1 = C_{\pi3} + C_{\pi4} + C_{cs1} + C_{cs3} \quad C_2 = C_{\pi6} + C_{cs2} + C_{cs4} \quad \text{and} \quad C_3 = C_L + C_{cs6} + C_{cs7} \]

Assuming the pole due to \( C_1 \) is much greater than the poles due to \( C_2 \) and \( C_3 \) gives,

The locations for the two poles are given by the following equations

\[ p'_1 = \frac{-1}{R_1 C_1} \quad \text{and} \quad p'_2 = \frac{-1}{R_{II} C_{II}} \]

where \( R_I (R_{II}) \) is the resistance to ground seen from the output of the first (second) stage and \( C_I (C_{II}) \) is the capacitance to ground seen from the output of the first (second) stage.
Uncompensated Frequency Response of an Op Amp

If we assume that $F(s) = 1$ (this is the worst case for stability considerations), then the above plot is the same as the loop gain.

Note that the phase margin is much less than 45°.

Therefore, the op amp must be compensated before using it in a closed-loop configuration.
MILLER COMPENSATION

Two-Stage Op Amp

The various capacitors are:

- $C_c$ = accomplishes the Miller compensation
- $C_M$ = capacitance associated with the first-stage mirror (mirror pole)
- $C_I$ = output capacitance to ground of the first-stage
- $C_{II}$ = output capacitance to ground of the second-stage
**Simplification of the Compensated Two-Stage, Small-Signal Frequency Response Model**

Use the CMOS op amp to illustrate:

1.) Assume that \( g_{m3} \gg g_{ds3} + g_{ds1} \)

2.) Assume that \( \frac{g_{m3}}{C_M} \gg GB \)

Therefore,

![Diagram of the simplified circuit](image)

Same circuit holds for the BJT op amp with different component relationships.
**General Two-Stage Frequency Response Analysis**

\[ V_{in} \rightarrow g_{ml}V_{in} \overset{C_{I}}{\rightarrow} R_I \overset{g_{ml}V_2}{\rightarrow} C_{II} \rightarrow V_{out} \]

Fig. 6.2-6

where

\[ g_{ml} = g_{m1} = g_{m2}, R_I = r_{ds2}||r_{ds4}, C_I = C_1 \]

and

\[ g_{mII} = g_{m6}, R_{II} = r_{ds6}||r_{ds7}, C_{II} = C_2 = C_L \]

Nodal Equations:

\[-g_{ml}V_{in} = [G_I + s(C_I + C_c)]V_2 - [sC_c]V_{out} \quad \text{and} \quad 0 = [g_{mII} - sC_c]V_2 + [G_{II} + sC_{II} + sC_c]V_{out}\]

Solving using Cramer’s rule gives,

\[
\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{ml}(g_{mII} - sC_c)}{G_I G_{II} + s [G_{II}(C_I + C_{II}) + G_I (C_{II} + C_c) + g_{mII} C_c] + s^2 [C_I C_{II} + C_c C_I + C_c C_{II}]} = A_o [1 - s (C_c / g_{mII})]
\]

where,

\[ A_o = g_{ml}g_{mII}R_I R_{II} \]

In general,

\[ D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s \left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \]

\[ \rightarrow D(s) \uparrow 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2}; \text{if} |p_2| >> |p_1| \]

\[ p_1 = \frac{-1}{R_I (C_I + C_{II}) + R_{II} (C_{II} + C_c) + g_{mII} R_I R_{II} C_c} \quad \uparrow \quad \frac{-1}{g_{mII} R_I R_{II} C_c}; \quad z = \frac{g_{mII}}{C_c} \]

\[ p_2 = \frac{-[R_I (C_I + C_{II}) + R_{II} (C_{II} + C_c) + g_{mII} R_I R_{II} C_c]}{R_I R_{II} (C_I C_{II} + C_c C_I + C_c C_{II})} \quad \uparrow \quad \frac{-g_{mII} C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \quad \uparrow \quad \frac{-g_{mII}}{C_{II}} \]

where \( C_{II} > C_c > C_I \).
Summary of Results for Miller Compensation of the Two-Stage Op Amp

There are three roots of importance:

1.) Right-half plane zero:

   This root is very undesirable because it boosts the loop magnitude while decreasing the phase.

2.) Dominant left-half plane pole (the Miller pole):

   \[ z_1 = \frac{g_mII}{C_c} = \frac{g_{m6}}{C_c} \]

   \[ p_1 = \frac{-1}{g_mII R_I R_{II} C_c} = \frac{-(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6} C_c} \]

   This root accomplishes the desired compensation.

3.) Left-half plane output pole:

   \[ p_2 = \frac{-g_mII}{C_{II}} \frac{-g_{m6}}{C_L} \]

   This pole must be beyond the unity-gainbandwidth or the phase margin will not be satisfied.

Root locus plot of the Miller compensation:

![Root locus plot](Fig. 6.2-7A)
Compensated Open-Loop Frequency Response of the Two-Stage Op Amp

Note that the unity-gainbandwidth, $GB$, is

$$GB = A_{vd}(0) \cdot |p_1| = \left( g_{ml}g_{mII}R_I R_{II} \right) \frac{1}{g_{mII} R_I R_{II} C_c} = \frac{g_{ml}}{C_c} + \frac{g_{m1}}{C_c} = \frac{g_{m2}}{C_c}$$

Fig. 6.2-7B
Conceptually, where do these roots come from?

1.) The Miller pole:

\[ |p_1| \sim \frac{1}{R_I(g_{m6}R_{II}C_c)} \]

2.) The left-half plane output pole:

\[ |p_2| \sim \frac{g_{m6}}{C_{II}} \]

3.) Right-half plane zero (Zeros always arise from multiple paths from the input to output):

\[ v_{out} = \left( \frac{-g_{m6}R_{II}(1/sC_c)}{R_{II} + 1/sC_c} \right)v' + \left( \frac{R_{II}}{R_{II} + 1/sC_c} \right)v'' = \frac{-R_{II}\left( \frac{g_{m6}}{sC_c} - 1 \right)}{R_{II} + 1/sC_c}v \]

where \( v = v' = v'' \).
Influence of the Mirror Pole

Up to this point, we have neglected the influence of the pole, $p_3$, associated with the current mirror of the input stage. If $|p_2| \approx |p_3|$, we have problems in compensation. This pole is given approximately as

$$p_3 \approx -\frac{g_{m3}}{C_M}$$

![Diagram showing open-loop and closed-loop poles with phase margin and gain-bandwidth product.](image-url)
Summary of the Conditions for Stability of the Two-Stage Op Amp (Assuming $p_2 \geq GB$

- Unity-gainbandwith is given as: 

$$GB = A_v(0)|p_1| = \left( g_{ml}g_{m2}R_1R_2 \right) \left( \frac{1}{g_{ml}R_1R_2C_c} \right) = \frac{g_m}{C_c} = (g_{m1}g_{m2}R_1R_2) \left( \frac{1}{g_{m2}R_1R_2C_c} \right) = \frac{g_m}{C_c}$$

- The requirement for $45^\circ$ phase margin is:

$$\pm 180^\circ - \text{Arg}[AF] = \pm 180^\circ - \tan^{-1}\left( \frac{\omega}{|p_1|} \right) - \tan^{-1}\left( \frac{\omega}{|p_2|} \right) - \tan^{-1}\left( \frac{\omega}{z} \right) = 45^\circ$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm 180^\circ - \tan^{-1}\left( \frac{GB}{|p_1|} \right) - \tan^{-1}\left( \frac{GB}{|p_2|} \right) - \tan^{-1}\left( \frac{GB}{z} \right) = 45^\circ$$

$$135^\circ \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left( \frac{GB}{|p_2|} \right) + \tan^{-1}(0.1) = 90^\circ + \tan^{-1}\left( \frac{GB}{|p_2|} \right) + 5.7^\circ$$

$$39.3^\circ \approx \tan^{-1}\left( \frac{GB}{|p_2|} \right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow |p_2| \leq 1.22GB$$

- The requirement for $60^\circ$ phase margin:

$$|p_2| \leq 2.2GB \text{ if } z \geq 10GB$$

- If $60^\circ$ phase margin is required, then the following relationships apply:

$$\frac{g_m}{C_c} > \frac{10g_m}{C_c} \Rightarrow g_m > 10g_m$$

$$\frac{g_m}{C_2} > \frac{2.2g_m}{C_c} \Rightarrow C_c > 0.22C_2$$
Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.

Solution of the problem:

If zeros are caused by two paths to the output, then eliminate one of the paths.
Use of Buffer to Eliminate the Feedforward Path through the Miller Capacitor

Model:

The transfer function is given by the following equation,

\[
\frac{V_o(s)}{V_{in}(s)} = \frac{(g_{ml})(g_{mII})(R_I)(R_{II})}{1 + s[R_I C_I + R_{II} C_{II} + R_I C_c + g_{ml} R_I R_{II} C_c] + s^2[R_I R_{II} C_{II}(C_I + C_c)]}
\]

Using the technique as before to approximate \( p_1 \) and \( p_2 \) results in the following

\[
p_1 \approx \frac{-1}{R_I C_I + R_{II} C_{II} + R_I C_c + g_{ml} R_I R_{II} C_c} \approx \frac{-1}{g_{ml} R_I R_{II} C_c}
\]

and

\[
p_2 \approx \frac{-g_{mII} C_c}{C_{II}(C_I + C_c)}
\]

Comments:

Poles are approximately what they were before with the zero removed.
For 45° phase margin, \(|p_2|\) must be greater than \( GB \)
For 60° phase margin, \(|p_2|\) must be greater than 1.73 \( GB \)
**Use of Buffer with Finite Output Resistance to Eliminate the RHP Zero**

Assume that the unity-gain buffer has an output resistance of $R_o$.

Model:

It can be shown that if the output resistance of the buffer amplifier, $R_o$, is not neglected that another pole occurs at,

$$p_4 \equiv \frac{-1}{R_o[C_1 C_c/(C_1 + C_c)]}$$

and a LHP zero at

$$z_2 \equiv \frac{-1}{R_o C_c}$$

Closer examination shows that if a resistor, called a *nulling resistor*, is placed in series with $C_c$ that the RHP zero can be eliminated or moved to the LHP.
Use of Nulling Resistor to Eliminate the RHP Zero (or turn it into a LHP zero)

![Nulling Resistor Diagram](image)

Nodal equations:

\[
g_{mI}V_{in} + \frac{V_I}{R_I} + sC_IV_I + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_I - V_{out}) = 0
\]

\[
g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_{out} + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_{out} - V_I) = 0
\]

Solution:

\[
\frac{V_{out}(s)}{V_{in}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_zC_c]\}}{1 + bs + cs^2 + ds^3}
\]

where

\[
a = g_{mI}g_{mII}R_I R_{II}
\]

\[
b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_I R_{II} C_c + R_z C_c
\]

\[
c = [R_I R_{II} (C_c C_{II} + C_I C_{II} + C_c C_{II}) + R_z C_c (R_I C_I + R_{II} C_{II})]
\]

\[
d = R_I R_{II} R_z C_I C_{II} C_c
\]

---

Use of Nulling Resistor to Eliminate the RHP - Continued

If $R_z$ is assumed to be less than $R_I$ or $R_{II}$ and the poles widely spaced, then the roots of the above transfer function can be approximated as

$$p_1 \approx \frac{-1}{(1 + g_{mII}R_{II})R_I C_c} \approx \frac{-1}{g_{mII}R_{II}R_I C_c}$$

$$p_2 \approx \frac{-g_{mII}C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \approx \frac{-g_{mII}}{C_{II}}$$

$$p_4 = \frac{-1}{R_z C_I}$$

and

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

Note that the zero can be placed anywhere on the real axis.
Conceptual Illustration of the Nulling Resistor Approach

The output voltage, $V_{out}$, can be written as

$$V_{out} = \frac{-g_{m6}R_I \left( R_z + \frac{1}{sC_c} \right) V'}{R_I + R_z + \frac{1}{sC_c}} + \frac{R_I}{R_I + R_z + \frac{1}{sC_c}} V' + \frac{-R_I \left[ g_{m6}R_z + \frac{g_{m6}}{sC_c} - 1 \right]}{R_I + R_z + \frac{1}{sC_c}} V''$$

when $V = V' = V''$.

Setting the numerator equal to zero and assuming $g_{m6} = g_{mII}$ gives,

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$
**A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, \( p_2 \)**

We desire that \( z_1 = p_2 \) in terms of the previous notation.

Therefore,

\[
\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}
\]

The value of \( R_z \) can be found as

\[
R_z = \left( \frac{C_c + C_{II}}{C_c} \right) (1/g_{mII})
\]

With \( p_2 \) canceled, the remaining roots are \( p_1 \) and \( p_4 \) (the pole due to \( R_z \)). For unity-gain stability, all that is required is that

\[
|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_I/C_c} = \frac{g_{mI}}{C_c}
\]

and

\[
\frac{1}{R_z C_I} > (g_{mI}/C_c) = GB
\]

Substituting \( R_z \) into the above inequality and assuming \( C_{II} >> C_c \) results in

\[
C_c > \sqrt{\frac{g_{mI}}{g_{mII} C_I C_{II}}}
\]

This procedure gives excellent stability for a fixed value of \( C_{II} (= C_L) \).

Unfortunately, as \( C_L \) changes, \( p_2 \) changes and the zero must be readjusted to cancel \( p_2 \).
**Increasing the Magnitude of the Output Pole**

The magnitude of the output pole, \( p_2 \), can be increased by introducing gain in the Miller capacitor feedback path. For example,

The resistors \( R_1 \) and \( R_2 \) are defined as

\[
R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \quad \text{and} \quad R_2 = \frac{1}{g_{ds6} + g_{ds7}}
\]

where transistors M2 and M4 are the output transistors of the first stage.

Nodal equations:

\[
I_{in} = G_1 V_1 - g_{m8} V_{s8} = G_1 V_1 - \left( \frac{g_{m8}sC_c}{g_{m8} + sC_c} \right) V_{out} \quad \text{and} \quad 0 = g_{m6} V_1 + \left[ G_2 + sC_2 + \frac{g_{m8}sC_c}{g_{m8} + sC_c} \right] V_{out}
\]

---

Increasing the Magnitude of the Output Pole - Continued

Solving for the transfer function $\frac{V_{out}}{I_{in}}$ gives,

$$
\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_{1}G_{2}}\right) \left[ \frac{1 + \frac{sC_{c}}{g_{m8}}}{1 + s\left(\frac{C_{c}}{g_{m8}} + \frac{C_{2}}{G_{2}} + \frac{C_{c}g_{m6}C_{c}}{G_{1}G_{2}} + s\left(\frac{C_{c}C_{2}}{g_{m8}G_{2}}\right)\right)} \right]
$$

Using the approximate method of solving for the roots of the denominator illustrated earlier gives

$$p_1 = \frac{-1}{\frac{C_{c}}{g_{m8}} + \frac{C_{c}}{G_{2}} + \frac{C_{2}}{G_{2}} + \frac{g_{m6}C_{c}}{G_{1}G_{2}}} = \frac{-6}{g_{m6}\cdot r_{ds}^{2}C_{c}}$$

and

$$p_2 = \frac{g_{m6}\cdot r_{ds}^{2}C_{c}}{6\cdot \frac{C_{c}C_{2}}{g_{m8}G_{2}}} = \frac{g_{m8}\cdot r_{ds}^{2}G_{2}\left(\frac{g_{m6}}{C_{2}}\right)}{6\cdot \left(\frac{g_{m8}\cdot r_{ds}}{3}\right)|p_2'|}$$

where all the various channel resistance have been assumed to equal $r_{ds}$ and $p_2'$ is the output pole for normal Miller compensation.

Result:

Dominant pole is approximately the same and the output pole is increased by roughly $g_{m}\cdot r_{ds}$. 
Concept Behind the Increasing of the Magnitude of the Output Pole

\[ |p_2| \approx \frac{g_{m6}g_{m8}r_{ds8}}{3C_\Pi} \]

Therefore, the output pole is approximately,

\[ R_{out} = r_{ds7}\left|\frac{3}{g_{m6}g_{m8}r_{ds8}}\right| \]

\[ \approx \frac{3}{g_{m6}g_{m8}r_{ds8}} \]

Therefore, the output pole is approximately,
FEEDFORWARD COMPENSATION

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

\[
\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}} \left( \frac{s + g_{miI}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]} \right)
\]

To use the LHP zero for compensation, a compromise must be observed.

- Placing the zero below \( GB \) will lead to boosting of the loop gain which could deteriorate the phase margin.
- Placing the zero above \( GB \) will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward compensation.
SELF-COMPENSATED OP AMPS

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback).

![Diagram](image)

Voltage gain:

\[
\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}
\]

Dominant pole:

\[
p_1 = -\frac{1}{R_{out}C_L}
\]

Unity-gainbandwidth:

\[
GB = A_v(0) \cdot |p_1| = \frac{G_m}{C_L}
\]

Stability:

Large load capacitors simply reduce the GB and the phase is 90° at the unity gain frequency.
**SIMPLE TWO-STAGE OP AMPS**

**BJT Two-Stage Op Amp**

Circuit:

![BJT Two-Stage Op Amp Circuit Diagram]

DC Conditions:

\[
I_5 = I_{bias}, \quad I_1 = I_2 = 0.5I_5 = 0.5I_{bias}, \quad I_7 = I_6 = nI_{bias}
\]

\[
V_{icm}(\text{max}) = V_{CC} - V_{EB3} - V_{CE1}(\text{sat}) + V_{BE1}
\]

\[
V_{icm}(\text{min}) = V_{EE} + V_{CE5}(\text{sat}) + V_{BE1}
\]

\[
V_{out}(\text{max}) = V_{CC} - V_{EC6}(\text{sat})
\]

\[
V_{out}(\text{min}) = V_{EE} + V_{CE7}(\text{sat})
\]

Notice that the output stage is class A \(\Rightarrow I_{sink} = I_7\) and \(I_{source} = \beta_F I_5 - I_7\)
Two-Stage BJT Op Amp - Continued

Small Signal Performance:

Assuming differential mode operation, we can write the small-signal model as,

\[
\begin{align*}
\text{v}_{\text{out}} &= \text{gm}_{1} \text{v}_{\text{in}} + \text{gm}_{2} \text{v}_{\text{in}} + \text{gm}_{4} \text{v}_{1} + \text{gm}_{6} \text{v}_{2} \\
\text{v}_{1} &= \frac{1}{\text{R}_{1}} \text{gm}_{1} \text{v}_{\text{in}} \\
\text{v}_{2} &= \frac{1}{\text{R}_{2}} \text{gm}_{6} \text{v}_{2} \\
\text{v}_{3} &= \frac{1}{\text{R}_{3}} \text{gm}_{4} \text{v}_{1} \\
\text{v}_{\text{out}} &= \text{C}_{c} \text{v}_{2}
\end{align*}
\]

where,

\[
R_{1} = \frac{1}{\text{g_{m3}}} \| r_{\pi3} \| r_{\pi4} \| r_{o3} \approx \frac{1}{\text{g_{m3}}} \quad R_{2} = r_{\pi6} \| r_{o2} \| r_{o4} \approx r_{\pi6} \quad \text{and} \quad R_{3} = r_{o6} \| r_{o7}
\]

\[
C_{1} = C_{\pi3} + C_{\pi4} + C_{cs1} + C_{cs3} \quad C_{2} = C_{\pi6} + C_{cs2} + C_{cs4} \quad \text{and} \quad C_{3} = C_{L} + C_{cs6} + C_{cs7}
\]

Note that we have ignored the base-collector capacitors, \( C_{\mu} \), except for M6, which is called \( C_{c} \).

Assuming the pole due to \( C_{1} \) is much greater than the poles due to \( C_{2} \) and \( C_{3} \) gives
Two-Stage BJT Op Amp - Continued

Summary of the small signal performance:

Midband performance-

\[ A_o = g_{m1}g_{mII}R_I R_{II} \approx g_{m1}g_{m6}r_\pi (r_{o6}||r_{o7}) = g_{m1}\beta_F (r_{o6}||r_{o7}), \quad R_{out} = r_{o6}||r_{o7}, \quad R_{in} = 2r_\pi \]

Roots-

Zero \( \approx \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c} \)

Poles at

\[ P_1 \approx -\frac{1}{g_{mII}R_I R_{II}C_c} \approx -\frac{1}{g_{m6}r_\pi (r_{o6}||r_{o7})C_c} = -\frac{g_{m1}}{A_o C_c} \] and \( P_2 \approx -\frac{g_{mII}}{C_{II}} -\frac{g_{m6}}{C_L} \)

Assume that \( \beta_F = 100, g_{m1} = 1\text{mS}, g_{m6} = 10\text{mS}, r_{o6} = r_{o7} = 0.5\text{M\Omega}, C_c = 5\text{pF} \) and \( C_L = 10\text{pF} \):

\[ A_o = (1\text{mS})(100)(250k\Omega) = 25,000\text{V/V}, \quad R_{in} = 2(\beta_F/g_{m1})2(100k\Omega) = 200k\Omega, \quad R_{out} = 250k\Omega \]

Zero \( \approx \frac{10\text{mS}}{5\text{pF}} = 2\times 10^9 \text{rads/sec or 318.3MHz} \),

\[ P_1 \approx \frac{-1\text{mS}}{(25,000)5\text{pF}} = -2\times 10^8 \text{ rads/sec or 1273Hz} \]

and \( P_2 \approx \frac{-10\text{mS}}{10\text{pF}} = 10^9 \text{ rads/sec or 159.15MHz} \)
Slew Rate of the Two-Stage BJT Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

\[ I_{\text{lim}} = C \frac{dv_C}{dt} \]

where \( v_C \) is the voltage across the capacitor \( C \).

Positive Slew Rate

\[ SR^+ = \min \left[ \frac{I_5}{C_c}, \frac{I_6-I_5-I_7}{C_L} \right] = \frac{I_5}{C_c} \]

because \( I_6 >> I_5 \)

Negative Slew Rate

\[ SR^- = \min \left[ \frac{I_5}{C_c}, \frac{I_7-I_5}{C_L} \right] = \frac{I_5}{C_c} \]

if \( I_7 >> I_5 \).

Therefore, if \( C_L \) is not too large and if \( I_7 \) is significantly greater than \( I_5 \), then the slew rate of the two-stage op amp should be,

\[ SR = \frac{I_5}{C_c} \]
Folded-Cascode BJT Op Amp

Circuit

DC Conditions:

\[ I_3 = I_{bias}, \quad I_1 = I_2 = 0.5I_5 = 0.5I_{bias}, \quad I_4 = I_5 = kI_{bias}, \quad I_{10} = I_{11} = kI_{bias} - 0.5I_{bias} \quad (k>1) \]

\[ V_{icm}(max) = V_{CC} - V_{CE3(sat)} + V_{EB1} \]

\[ V_{icm}(min) = V_{EE} + V_{CE4(sat)} + V_{EC1(sat)} - V_{BE1} \]

\[ V_{out}(max) = V_{CC} - V_{EC9(sat)} - V_{EC11(sat)} \]

\[ V_{out}(min) = V_{EE} + V_{CE5(sat)} + V_{CE7(sat)} \]

Notice that the output stage is push-pull \( \Rightarrow I_{sink} \) and \( I_{source} \) are limited by the base current.
Folded-Cascode BJT Op Amp - Continued

Small-Signal Analysis:

\[
\frac{g_{m1}v_{in}}{2} r_{o1} \quad r_{o4} \quad r_{\pi 6} \quad v_{be6} \quad r_{o6} \quad 1 \quad g_{m10} \quad \frac{g_{m2}v_{in}}{2} r_{o2} \quad r_{o5} \quad r_{\pi 7} \quad v_{be7} \quad r_{o7} \quad i_{10} \quad g_{m7}v_{be7} \quad R_B \quad i_7 \quad \beta r_{o11} \quad v_{out} \quad OA09
\]

where \( R_A \approx \frac{1}{g_{m6}} \) and \( R_B \approx \frac{r_{\pi 7} + \beta p r_{o11}/2}{1 + g_{m7} r_{o7}} \) if \( r_{o7} \approx r_{o11} \)

\[
i_{10} \approx -\frac{g_{m1} r_{\pi 6} v_{in}}{2 (r_{\pi 6} + R_A)} \quad \frac{-g_{m1} v_{in}}{2}
\]

\[
i_7 \approx \frac{g_{m2} r_{\pi 7} v_{in}}{2 (r_{\pi 7} + R_B)} \quad \frac{g_{m2} r_{\pi 7} v_{in}}{2 (r_{\pi 7} + 0.5 r_{\pi 7})} = \frac{g_{m2} v_{in}}{3}
\]

\[\therefore v_{out} = (i_7 - i_{10}) \beta p R_{out} v_{in} = \frac{5}{6} (g_{m1} \beta p R_{out}) v_{in} \quad \text{if } g_{m1} = g_{m2} \Rightarrow \frac{v_{out}}{v_{in}} = \frac{5}{6} (g_{m1} \beta p R_{out})
\]

\[R_{out} = \beta p r_{o11} \parallel [\beta_N (r_{o5} \parallel r_{o2})] \quad \text{and} \quad R_{in} = 2 \pi_1
\]

Assume that \( \beta_{FN} = 100, \ \beta_{FP} = 50, \ g_{m1} = g_{m2} = 1 \text{mS}, \ r_{oN} = 1 \text{M} \Omega, \) and \( r_{oP} = 0.5 \text{M} \Omega: \)

\[\frac{v_{out}}{v_{in}} = 14.285 \text{V/V} \quad R_{out} = 14.285 \text{ M} \Omega \quad \text{and} \quad R_{in} = 100 \text{k} \Omega\]
**Folded-Cascode BJT Op Amp - Continued**

Frequency response includes only 1 dominant pole at the output (self-compensation),

\[ p_1 = \frac{-1}{R_{out} C_L} \]

There are other poles but we shall assume that they are less than \( GB \)

If \( C_L = 25 \text{pF} \), then \(|p_1| = 2800 \text{ rads/sec. or 446Hz} \implies GB = 6.371 \text{ MHz} \)

Checking some of the nondominant poles gives:

\[ |p_A| = \frac{1}{R_A C_A} = \frac{g_{m6}}{C_A} \implies 159 \text{MHz if } C_A = 1 \text{pf} \text{ (the capacitance to ac ground at the emitter of Q6)} \]

\[ |p_B| = \frac{1}{R_B C_B} = \frac{2}{r_{\pi7} C_B} \implies 6.37 \text{MHz if } C_B = 1 \text{pf} \text{ (the capacitance to ac ground at the emitter of Q7)} \]

This indicates that for small capacitive loads, this op amp will suffer from higher poles with respect to phase margin. Capacitive loads greater than 25pF, will have better stability (and less \( GB \)).
Two-Stage CMOS Op Amp

Circuit:

DC Conditions:

\[ I_5 = I_{bias}, \quad I_1 = I_2 = 0.5I_5 = 0.5I_{bias}, \quad I_7 = I_6 = nI_{Bias} \]

\[ V_{icm}(\text{max}) = V_{DD} - V_{SG3} + V_{T1} \]

\[ V_{icm}(\text{min}) = V_{SS} + V_{DS5}^{\text{sat}} + V_{GS1} \]

\[ V_{out}(\text{max}) = V_{DD} - V_{SD6}^{\text{sat}} \]

\[ V_{out}(\text{min}) = V_{SS} + V_{DS7}^{\text{sat}} \]

Notice that the output stage is class A \( \Rightarrow I_{sink} = I_7 \) and \( I_{source} = \frac{K_N W_6}{2L_6} (V_{DD} - V_{SS} - V_T)^2 - I_7 \)
**DC Balance Conditions for the Two-Stage Op Amp**

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

1.) First assume that $V_{SG4} = V_{SG6}$. This will cause “proper mirroring” in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is “guaranteed” to be in saturation.

2.) Let $S_i \equiv \frac{W_i}{L_i}$, if $V_{SG4} = V_{SG6}$, then $I_6 = \left( \frac{S_6}{S_4} \right) I_4$

3.) However, $I_7 = \left( \frac{S_7}{S_5} \right) I_5 = \left( \frac{S_7}{S_5} \right) (2I_4)$

4.) For balance, $I_6$ must equal $I_7$ ⇒ $\frac{S_6}{S_4} = \frac{2S_7}{S_5}$ which is called the “balance conditions”

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.
Small-Signal Performance of the Two-Stage CMOS Op Amp

Summary of the small signal performance:

- $g_mV_{in} > g_{ds2} + g_{ds4}$
- $g_m > GB$
- $C_M > GB$
Midband performance-

\[ A_o = g_{m1} g_{mII} R_I R_{II} \approx g_{m1} g_{m6} (r_{ds2} || r_{ds4}) (r_{ds6} || r_{ds7}) \]
\[ R_{out} = r_{ds6} || r_{ds7}, \quad R_{in} = \infty \]

Roots-

Zero = \( \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c} \)

Poles at
\[ p_1 = -\frac{-1}{g_{mII} R_I R_{II} C_c} \frac{(g_{ds2} + g_{ds4}) (g_{ds6} + g_{ds7})}{g_{m6} C_c} \]
\[ p_2 = \frac{-g_{mII}}{C_{II}} \frac{-g_{m6}}{C_L} \]

Assume that \( g_{m1} = 100\mu S, g_{m6} = 1mS, r_{ds2} = r_{ds4} = 2\Omega, r_{ds6} = r_{ds7} = 0.5\Omega, C_c = 5pF \text{ and } C_L = 10pF: \)

\[ A_o = (100\mu S)(1\Omega)(1000\mu S)(0.25\Omega) = 25,000V/V, \quad R_{in} = \infty, \quad R_{out} = 250k\Omega \]

Zero = \( \frac{1000\mu S}{5pF} = 2\times10^8 \text{ rads/sec or 31.83MHz} \),

\[ p_1 = \frac{-1}{(1mS)(1\Omega)(0.25\Omega)(5pF)} = -800 \text{ rads/sec or 127.3Hz}, \quad GB = 3.178MHz \]

and \[ p_2 = \frac{-1000\mu S}{10pF} = 10^8 \text{ rads/sec or 15.915MHz} \]
**Slew Rate of a Two-Stage CMOS Op Amp**

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

\[ I_{\text{lim}} = C \frac{dv_C}{dt} \]

where \( v_C \) is the voltage across the capacitor \( C \).

\( \text{Assume a virtual ground} \)

\[ v_{\text{in}} >> 0 \]

\[ v_{\text{in}} << 0 \]

\[ v_{\text{in}} = 0 \]

\[ v_{\text{out}} \]

\[ V_{DD} \]

\[ V_{SS} \]

\[ V_{Bias} \]

\[ C \]

\[ I \]

\[ I_{\text{5}} \]

\[ I_{\text{6}} \]

\[ I_{\text{7}} \]

\[ I_{\text{CL}} \]

\[ I_{\text{ICL}} \]

\[ C_L \]

\[ C_c \]

\[ SR^+ = \min \left[ \frac{I_{\text{5}}}{C_c}, \frac{I_{\text{6}} - I_{\text{5}} - I_{\text{7}}}{C_L} \right] = \frac{I_{\text{5}}}{C_c} \quad \text{because} \quad I_{\text{6}} >> I_{\text{5}} \]

\[ SR^- = \min \left[ \frac{I_{\text{5}}}{C_c}, \frac{I_{\text{7}} - I_{\text{5}}}{C_L} \right] = \frac{I_{\text{5}}}{C_c} \quad \text{if} \quad I_{\text{7}} >> I_{\text{5}}. \]

Therefore, if \( C_L \) is not too large and if \( I_{\text{7}} \) is significantly greater than \( I_{\text{5}} \), then the slew rate of the two-stage op amp should be,

\[ SR = \frac{I_{\text{5}}}{C_c} \]

**Folded Cascode, CMOS Op Amp**
Comments:
• The bias currents, $I_4$ and $I_5$, should be designed so that $I_6$ and $I_7$ never become zero (i.e. $I_5=I_6=1.5I_3$)
• This amplifier is nearly balanced (would be exactly if $R_A$ was equal to $R_B$)
• Self compensating
• Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if $R_A$ and $R_B$ are greater than $g_{m1}$ or $g_{m2}$.)
Small-Signal Analysis of the Folded Cascode Op Amp

Model:

Recalling what we learned about the resistance looking into the source of the cascode transistor,

\[ R_A = \frac{r_{ds6} + R_2 + (1/g_m10)}{1 + g_m6r_{gs6}} \frac{1}{g_m6} \]

and

\[ R_B = \frac{r_{ds7} + R_{II}}{1 + g_m7r_{ds7}} \frac{R_{II}}{g_m7r_{ds7}} \]

where \( R_{II} = g_m9r_{ds9}r_{ds11} \)

The small-signal voltage transfer function can be found as follows. The current \( i_{10} \) is written as

\[ i_{10} = \frac{-g_m1(r_{ds1}||r_{ds4})v_{in1}}{2[R_A + (r_{ds1}||r_{ds4})]} \frac{-g_m1v_{in1}}{2} \]

and the current \( i_7 \) can be expressed as

\[ i_7 = \frac{g_m2(r_{ds2}||r_{ds5})v_{in}}{2\left[\frac{R_{II}}{g_m7r_{ds7}} + (r_{ds2}||r_{ds5})\right]} = \frac{g_m2v_{in}}{2(1+k)} \]

where \( k = \frac{R_{II}(g_{ds2} + g_{ds4})}{g_m7r_{ds7}} \)

The output voltage, \( v_{out} \), is equal to the sum of \( i_7 \) and \( i_{10} \) flowing through \( R_{out} \). Thus,

\[ \frac{v_{out}}{v_{in}} = \left(\frac{g_m1}{2} + \frac{g_m2}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)g_mR_{out} \]
**Frequency Response of the Folded Cascode Op Amp**

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as:

\[
p_{out} = \frac{-1}{R_{out}C_{out}}
\]

where \( C_{out} \) is all the capacitance connected from the output of the op amp to ground.

All other poles must be greater than \( GB = \frac{g_{m1}}{C_{out}} \). The approximate expressions for each pole is:

1.) Pole at node A:
\[
p_A \propto -\frac{1}{R_A C_A}
\]

2.) Pole at node B:
\[
p_B \propto -\frac{1}{R_B C_B}
\]

3.) Pole at drain of M6:
\[
p_6 \propto -\frac{1}{(R_2 + 1/g_{m10}) C_6}
\]

4.) Pole at source of M8: \( p_8 \propto -\frac{g_{m8}}{C_8} \)

5.) Pole at source of M9: \( p_9 \propto -\frac{g_{m9}}{C_9} \)

6.) Pole at gate of M10:
\[
p_{10} \propto -\frac{g_{m10}}{C_{10}}
\]

where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because \( R_B \) is approximately \( r_{ds} \) that this pole might be too small. However, at frequencies where this pole has influence, \( C_{out} \), causes \( R_{out} \) to be much smaller making \( p_B \) also non-dominant.
Folded Cascode, CMOS Op Amp - Example

Assume that all $g_{mn} = g_{mp} = 100 \mu S$, $r_{dsN} = 2 \Omega$, $r_{dsP} = 1 \Omega$, and $C_L = 10 \text{pF}$. Find all of the small-signal performance values for the folded-cascode op amp.

$R_{II} = 0.4 \Omega$, $R_A = 10 \Omega$, and $R_B = 4 \Omega$  \[ k = \frac{0.4 \times 10^9 (0.3 \times 10^{-6})}{100} = 1.2 \]

$\frac{v_{out}}{v_{in}} = \left(\frac{2+1.2}{2+2.2}\right) (100)(57.143) = 4.354 \text{V/V}$

$R_{out} = R_{II} \left| \left[ \frac{g_m r_{dsP}}{ (r_{dsP} || r_{dsN}) } \right] \right| = 400 \Omega \left| \left[ (100)(0.667 \Omega) \right] \right| = 57.143 \Omega$

$|P_{out}| = \frac{1}{R_{out} C_{out}} = \frac{1}{57.143 \Omega \cdot 10 \text{pF}} = 1.750 \text{rads/sec.} \Rightarrow 278 \text{Hz} \Rightarrow GB = 1.21 \text{MHz}$

Comments on the Folded Cascode, CMOS Op Amp:

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required
OP AMP DESIGN

Unbuffered, Two-Stage CMOS Op Amp

![Circuit Diagram](image_url)

Notation:

\[ S_i = \frac{W_i}{L_i} = W/L \text{ of the } i\text{th transistor} \]
Design Relationships for the Two-Stage Op Amp

Slew rate \( SR = \frac{I_5}{C_c} \) (Assuming \( I_7 >> I_5 \) and \( C_L > C_c \))

First-stage gain \( A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \)

Second-stage gain \( A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)} \)

Gain-bandwidth \( GB = \frac{g_{m1}}{C_c} \)

Output pole \( p_2 = \frac{-g_{m6}}{C_L} \)

RHP zero \( z_1 = \frac{g_{m6}}{C_c} \)

\( 60^\circ \) phase margin requires that \( g_{m6} = 2.2g_{m2}(C_L/C_c) \) if all other roots are \( \geq 10GB \).

Positive ICMR \( V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{(max)} + V_{T1(min)} \)

Negative ICMR \( V_{in(min)} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(max)} + V_{DS5(sat)} \)

Saturation voltage \( V_{DS(sat)} = \sqrt{\frac{2I_{DS}}{\beta}} \)

It is assumed that all transistors are in saturation for the above relationships.
**Op Amp Specifications**

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, $GB$
3. Phase margin (or settling time)
4. Input common-mode range, $ICMR$
5. Load Capacitance, $C_L$
6. Slew-rate, $SR$
7. Output voltage swing
8. Power dissipation, $P_{diss}$

![Op Amp Diagram](image-url)
Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc \((A_v)\), unity gain bandwidth \((GB)\), input common mode range \((V_{in}(\text{min}) \text{ and } V_{in}(\text{max}))\), load capacitance \((C_L)\), slew rate \((SR)\), settling time \((T_s)\), output voltage swing \((V_{out}(\text{max}) \text{ and } V_{out}(\text{min}))\), and power dissipation \((P_{diss})\) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for \(C_c\), i.e. for a 60° phase margin we use the following relationship. This assumes that \(z \geq 10GB\).
   \[
   C_c > 0.22C_L
   \]

2. Determine the minimum value for the “tail current” \(I_5\) from the largest of the two values.
   \[
   I_5 = SR \cdot C_c \\
   \text{or} \\
   I_5 \equiv 10 \left( \frac{V_{DD} + |V_{SS}|}{2 \cdot T_s} \right)
   \]

3. Design for \(S_3\) from the maximum input voltage specification.
   \[
   S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\text{max}) - |V_{T03}|(\text{max}) + V_{T1}(\text{min})]^2} \geq 1
   \]

4. Verify that the pole of M3 due to \(C_{gs3}\) and \(C_{gs4} (=0.67W_3L_3C_{ox})\) will not be dominant by assuming it to be greater than 10 \(GB\).
   \[
   \frac{g_{m3}}{2C_{gs3}} > 10GB.
   \]

5. Design for \(S_1 \text{ (} S_2 \text{)}\) to achieve the desired \(GB\).
   \[
   g_{m1} = GB \cdot C_c \Rightarrow S_2 = \frac{g_{m2}}{K'_2I_5}
   \]
Unbuffered Op Amp Design Procedure - Continued

6. Design for $S_5$ from the minimum input voltage. First calculate $V_{DS5(sat)}$ then find $S_5$.

$$V_{DS5(sat)} = V_{in(min)} - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1(max)} \geq 100 \text{ mV} \rightarrow S_5 = \frac{2I_5}{K_5[V_{DS5(sat)}]^2}$$

7. Find $S_6$ by letting the second pole ($p_2$) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$g_{m6} = 2.2g_{m2}(C_L/C_c) \rightarrow S_6 = S_4 \frac{g_{m6}}{g_{m4}}$$

8. Calculate $I_6$ from

$$I_6 = \frac{g_{m6}^2}{2K_6S_6}$$

Check to make sure that $S_6$ satisfies the $V_{out(max)}$ requirement and adjust as necessary.

9. Design $S_7$ to achieve the desired current ratios between $I_5$ and $I_6$.

$$S_7 = (I_6/I_5)S_5$$ (Check the minimum output voltage requirements)

10. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, $I_5$ and $I_6$, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents $I_5$ and $I_6$. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.
Example 6.3-1 - Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1µm.

\[ A_v > 3000 \text{V/V} \quad V_{DD} = 2.5 \text{V} \quad V_{SS} = -2.5 \text{V} \quad 60^\circ \text{phase margin} \]

\[ GB = 5 \text{MHz} \quad C_L = 10 \text{pF} \quad SR > 10 \text{V/µs} \]

\[ V_{out} \text{ range} = \pm 2 \text{V} \quad ICMR = -1 \text{ to 2 V} \quad P_{diss} \leq 2 \text{mW} \]

**Solution**

1.) The first step is to calculate the minimum value of the compensation capacitor \( C_c \), which is

\[ C_c > (2.2/10)(10 \text{ pF}) = 2.2 \text{ pF} \]

2.) Choose \( C_c \) as 3pF. Using the slew-rate specification and \( C_c \) calculate \( I_5 \).

\[ I_5 = (3 \times 10^{-12})(10 \times 10^6) = 30 \mu\text{A} \]

3.) Next calculate \((W/L)_3\) using ICMR requirements.

\[ (W/L)_3 = \frac{30 \times 10^{-6}}{(50 \times 10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 3 \quad \rightarrow \quad (W/L)_3 = (W/L)_4 = 3 \]

4.) Now we can check the value of the mirror pole, \( p_3 \), to make sure that it is in fact greater than 10\( GB \). Assume the \( C_{ox} = 0.4 \text{fF/µm}^2 \). The mirror pole can be found as

\[ p_3 \cdot \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = 6.79 \times 10^9(\text{rads/sec}) \]

or 1.08 GHz. Thus, \( p_3 \), is not of concern in this design because \( p_3 >> 10GB \).
Example 6.3-1 - Continued

5.) The next step in the design is to calculate $g_{m1}$ to get

$$g_{m1} = (5 \times 10^6)(2\pi)(3 \times 10^{-12}) = 94.25 \mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K'N_1} = \frac{(94.25)^2}{2 \cdot 110 \cdot 15} = 2.79 \approx 3.0 \Rightarrow (W/L)_1 = (W/L)_2 = 3$$

6.) Next calculate $V_{DS5}$,

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30 \times 10^{-6}}{110 \times 10^{-6} \cdot 0.35}} - 0.85 = 0.35 \text{V}$$

Using $V_{DS5}$ calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30 \times 10^{-6})}{(110 \times 10^{-6})(0.35)^2} = 4.49 \approx 4.5 \Rightarrow (W/L)_5 = 4.5$$

7.) For $60^\circ$ phase margin, we know that

$$g_{m6} \geq 10g_{m1} \geq 942.5 \mu\text{S}$$

Assuming that $g_{m6} = 942.5 \mu\text{S}$ and knowing that $g_{m4} = 67 \mu\text{S}$, we calculate $(W/L)_6$ as

$$(W/L)_6 = 3 \frac{942.5 \times 10^{-6}}{67 \times 10^{-6}} = 42.2 \approx 40$$
**Example 6.3-1 - Continued**

8.) Calculate $I_6$ using the small-signal $g_m$ expression:

$$I_6 = \frac{(942.5 \times 10^{-6})^2}{(2)(50 \times 10^{-6})(42)} = 211.5 \mu A \approx 212 \mu A$$

If we calculate $(W/L)_6$ based on $V_{out}(\text{max})$, the value is approximately 38. Since 42 exceeds the specification and maintains better phase margin, we will stay with $(W/L)_6 = 42$ and $I_6 = 212 \mu A$.

With $I_6 = 212 \mu A$ the power dissipation is

$$P_{diss} = 5V \cdot (30 \mu A + 212 \mu A) = 1.21 \text{mW}.$$  

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5 \left( \frac{234 \times 10^{-6}}{30 \times 10^{-6}} \right) = 35.1 \approx 35 \quad \rightarrow \quad (W/L)_7 = 35$$

Let us check the $V_{out}(\text{min})$ specification although the W/L of M7 is so large that this is probably not necessary. The value of $V_{out}(\text{min})$ is

$$V_{out}(\text{min}) = V_{DS7(\text{sat})} = \sqrt{\frac{2 \cdot 234}{110 \cdot 35}} = 0.349V$$

which is less than required. At this point, the first-cut design is complete.

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(92.45 \times 10^{-6})(942.5 \times 10^{-6})}{15 \times 10^{-6}(0.04 + 0.05)212 \times 10^{-6}(0.04 + 0.05)} = 3,383 V/V$$

which barely meets specifications. We might want to consider decreasing the output current back to 190\(\mu A\) to increase the second-stage gain by a factor of 1.1 or better yet, increase the channel length to 2\(\mu m\) causing a gain increase of 20.
Incorporating the Nulling Resistor into the Miller Compensated Two-Stage Op Amp Circuit:

We saw earlier that the roots were:

\[ p_1 = -\frac{g_{m2}}{A_v C_C} = -\frac{g_{m1}}{A_v C_C} \quad p_2 = -\frac{g_{m6}}{C_L} \]

\[ p_3 = -\frac{1}{R_z C_f} \quad z_1 = \frac{-1}{R_z C_C - C_C/g_{m6}} \]

where \( A_v = g_{m1}g_{m6}R_1R_{II} \). (Note that \( p_3 \) is the pole resulting from the nulling resistor compensation technique.)
**Design of the Nulling Resistor (M8)**

In order to place the zero on top of the second pole \((p_2)\), the following relationship must hold

\[
R_z = \frac{1}{g_{m6}} \left( \frac{C_L + C_c}{C_c} \right) = \left( \frac{C_c + C_L}{C_c} \right) \frac{1}{\sqrt{2K'_{PS}I_6}}
\]

The resistor, \(R_z\), is realized by the transistor M8 which is operating in the active region because the dc current through it is zero. Therefore, \(R_z\), can be written as

\[
R_z = \frac{v_{DS8}}{i_{D8}} = \frac{1}{K'_{PS8}(V_{SG8} - |V_{TP}|)}
\]

The bias circuit is designed so that voltage \(V_A\) is equal to \(V_B\).

\[
|V_{GS10}| - |V_I| = |V_{GS8}| - |V_I| \quad \Rightarrow \quad V_{SG11} = V_{SG6} \quad \Rightarrow \quad \left( \frac{W_{11}}{L_{11}} \right) = \left( \frac{I_{10}}{I_6} \right) \left( \frac{W_6}{L_6} \right)
\]

In the saturation region

\[
|V_{GS10}| - |V_I| = \sqrt{\frac{2(I_{10})}{K'_{P}(W_{10}/L_{10})}} = |V_{GS8}| - |V_I|
\]

\[
R_z = \frac{1}{K'_{PS8}} \sqrt{\frac{K'_{PS10}}{2I_{10}}} = \frac{1}{S_8} \sqrt{\frac{S_{10}}{2K'_{PS10}}}
\]

Equating the two expressions for \(R_z\) gives

\[
\left( \frac{W_8}{L_8} \right) = \left( \frac{C_c}{C_L + C_c} \right) \sqrt{\frac{S_{10}S_6I_6}{I_{10}}}
\]
Example 6.3-2 - RHP Zero Compensation

Use results of Ex. 6.3-1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole $p_2$. Use device data given in Ex. 6.3-1.

**Solution**

The task at hand is the design of transistors M8, M9, M10, M11, and bias current $I_{10}$. The first step in this design is to establish the bias components. In order to set $V_A$ equal to $V_B$, then $V_{SG10}$ must equal $V_{SG6}$. Therefore,

$$S_{11} = \left( \frac{I_{11}}{I_6} \right) S_6$$

Choose $I_{11} = I_{10} = I_9 = 30\mu A$ which gives $S_{11} = (30\mu A/212\mu A)42 = 5.94 \approx 6$.

$$W_{11} = 6\mu m$$

The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of $V_{SG11}$, $V_{SG10}$, and $V_{DS9}$. The ratio of $I_{10}/I_5$ determines the $(W/L)$ of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (30/30)(4.5) = 4.5$$

$$W_9 = 4.5\mu m$$

Now $(W/L)_8$ is determined to be

$$(W/L)_8 = \left( \frac{3pF}{3pF+10pF} \right) \sqrt{1.42 \cdot 212\mu A / 30\mu A} = 3.98$$

$$W_8 = 3.98\mu m \approx 4\mu m$$
**Example 6.3-2 - Continued**

It is worthwhile to check that the RHP zero has been moved on top of $p_2$. To do this, first calculate the value of $R_z$. $V_{SG8}$ must first be determined. It is equal to $V_{SG10}$, which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K_pS_{10}}} + |V_{TP}| = \sqrt{\frac{2\cdot30}{50\cdot1}} + 0.7 = 1.795\text{V}$$

Next determine $R_z$.

$$R_z = \frac{1}{K_pS_8(V_{SG10}-|V_{TP}|)} = \frac{10^6}{50\cdot3.97(1.795-0.7)} = 4.601\text{k}\Omega$$

The location of $z_1$ is calculated as

$$z_1 = \frac{-1}{(4.601 \times 10^3)(3\times10^{-12}) - \frac{3\times10^{-12}}{942.5\times10^{-6}}} = -94.16\times10^6 \text{ rads/sec}$$

The output pole, $p_2$, is

$$p_2 = \frac{942.5\times10^{-6}}{10\times10^{-12}} = -94.25\times10^6 \text{ rads/sec}$$

Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below.

$W_8 = 4\mu\text{m} \quad W_9 = 4.5\mu\text{m} \quad W_{10} = 1\mu\text{m} \quad W_{11} = 6\mu\text{m}$
**An Alternate Form of Nulling Resistor**

To cancel $p_2$,

$$z_1 = p_2 \rightarrow R_z = \frac{C_c + C_L}{g_{m6A}C_c} = \frac{1}{g_{m6B}}$$

Which gives

$$g_{m6B} = g_{m6A} \left( \frac{C_c}{C_c + C_L} \right)$$

In the previous example,

$$g_{m6A} = 942.5 \mu S, C_c = 3pF \text{ and } C_L = 10pF.$$  

Choose $I_{6B} = 10\mu A$ to get

$$g_{m6B} = \frac{g_{m6A}C_c}{C_c + C_L} \rightarrow \sqrt{\frac{2KPW_{6B}I_{6B}}{L_{6B}}} = \left( \frac{C_c}{C_c + C_L} \right) \sqrt{\frac{2KPW_{6A}I_{6D}}{L_{6A}}}$$

or

$$\frac{W_{6B}}{L_{6B}} = \left( \frac{3}{13} \right)^2 \frac{I_{6A}}{I_{6B}} \cdot \frac{W_{6A}}{L_{6A}} = \left( \frac{3}{13} \right)^2 \left( \frac{234}{10} \right)^{23} = 28.7 \rightarrow W_{6B} = 29\mu m$$
Implementation of $C_c$ using a MOS Transistor

Two Approaches:
1.) Have to keep $V_{GS} \geq V_T$

2.) Better - $V_{GS}$ not restricted
**Programmability of the Two-Stage Op Amp**

The following relationships depend on the bias current, $I_{bias}$, in the following manner and allow for programmability after fabrication.

\[ A_v(0) = g_{ml}g_{mII}R_I R_{II} \propto \frac{1}{I_{Bias}} \]

\[ GB = \frac{g_{ml}}{C_c} \propto \sqrt{I_{Bias}} \]

\[ P_{diss} = (V_{DD} + |V_{SS}|)(1+K_1+K_2)I_{Bias} \propto I_{bias} \]

\[ SR = \frac{K_1I_{Bias}}{C_c} \propto I_{Bias} \]

\[ R_{out} = \frac{1}{2\lambda K_2I_{Bias}} \propto \frac{1}{I_{Bias}} \]

\[ |p_1| = \frac{1}{g_{mII}R_I R_{II}C_c} \propto \frac{I_{Bias}^2}{\sqrt{I_{Bias}}} \propto I_{Bias}^{1.5} \]

\[ |z| = \frac{g_{mII}}{C_c} \propto \sqrt{I_{Bias}} \]

Illustration of the $I_{bias}$ dependence →

![Fig. 6.3-04D](image)

![Fig. 6.3-4E](image)
**Simulation of the Electrical Design**

Area of source or drain = \( AS = AD = W[L_1 + L_2 + L_3] \)

where

- \( L_1 = \) Minimum allowable distance between the contact in the S/D and the polysilicon (5\(\mu\)m)
- \( L_2 = \) Width of a minimum size contact (5\(\mu\)m)
- \( L_3 = \) Minimum allowable distance from the contact in S/D to the edge of the S/D (5\(\mu\)m)

\[ \therefore AS = AD = W \times 15\mu m \]

Perimeter of the source or drain = \( PD = PS = 2W + 2(L_1 + L_2 + L_3) \)

\[ \therefore PD = PS = 2W + 30\mu m \]

Illustration:
Reduction of Parasitics

The major objective of good layout is to minimize the parasitics that influence the design.

Typical parasitics include:

- Capacitors to ac ground
- Series resistance

Capacitive parasitics is minimized by minimizing area and maximizing the distance between the conductor and ac ground.

Resistance parasitics are minimized by using wide busses and keeping the bus length short.

For example:

At 2mΩ/square, a metal run of 1000μm and 2μm wide will have 1Ω of resistance.

At 1 mA this amounts to a 1 mV drop which could easily be greater than the least significant bit of an analog-digital converter. (For example, a 10 bit ADC with $V_{REF} = 1$V has an LSB of 1mV)
SUMMARY

Introduction and Characterization

• Ideal op amp, virtual ground at input when gain approaches infinity
• Characteristics are static and dynamic and time-independent and time-dependent

Op Amp Architectures

• Two stage
• Folded
• Many others

Compensation

• Designed so that the op amp with unity gain feedback (buffer) is stable
• Types
  - Miller
  - Miller with nulling resistors
  - Self Compensating
  - Feedforward

Simple Op Amps

• CMOS - two-stage and folded cascode
• BJT - two-stage and folded cascode

Op Amp Design

• CMOS only